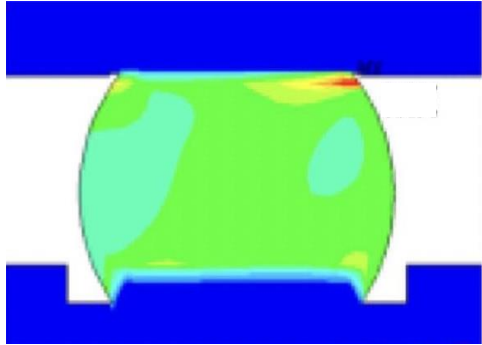
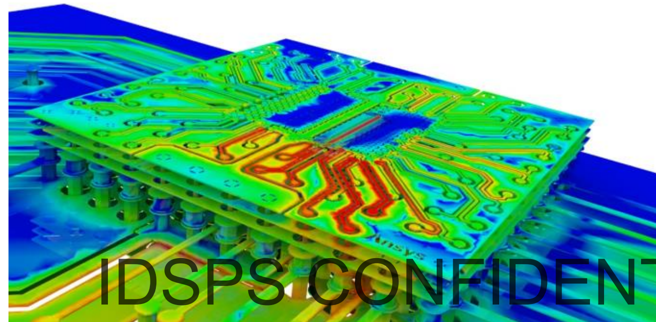
Predictive Modeling and Co-design

Industry Co-development Centre for the Next-generation Research and Workforce



Tarun Agarwal, EE, IIT Gandhinagar (Lead)
Somnath Roy, ME, IIT Kharagpur (Co-lead)
&
Anil Kumar, ANSYS (Industry Lead)
Parthasarathy Ramaswamy, Intel (Industry Co-lead)

&
Global Academic Collaborators
Prof. Abhijit Dasgupta, University of Maryland, USA
Prof. Ganesh Subbarayan, Purdue University, USA

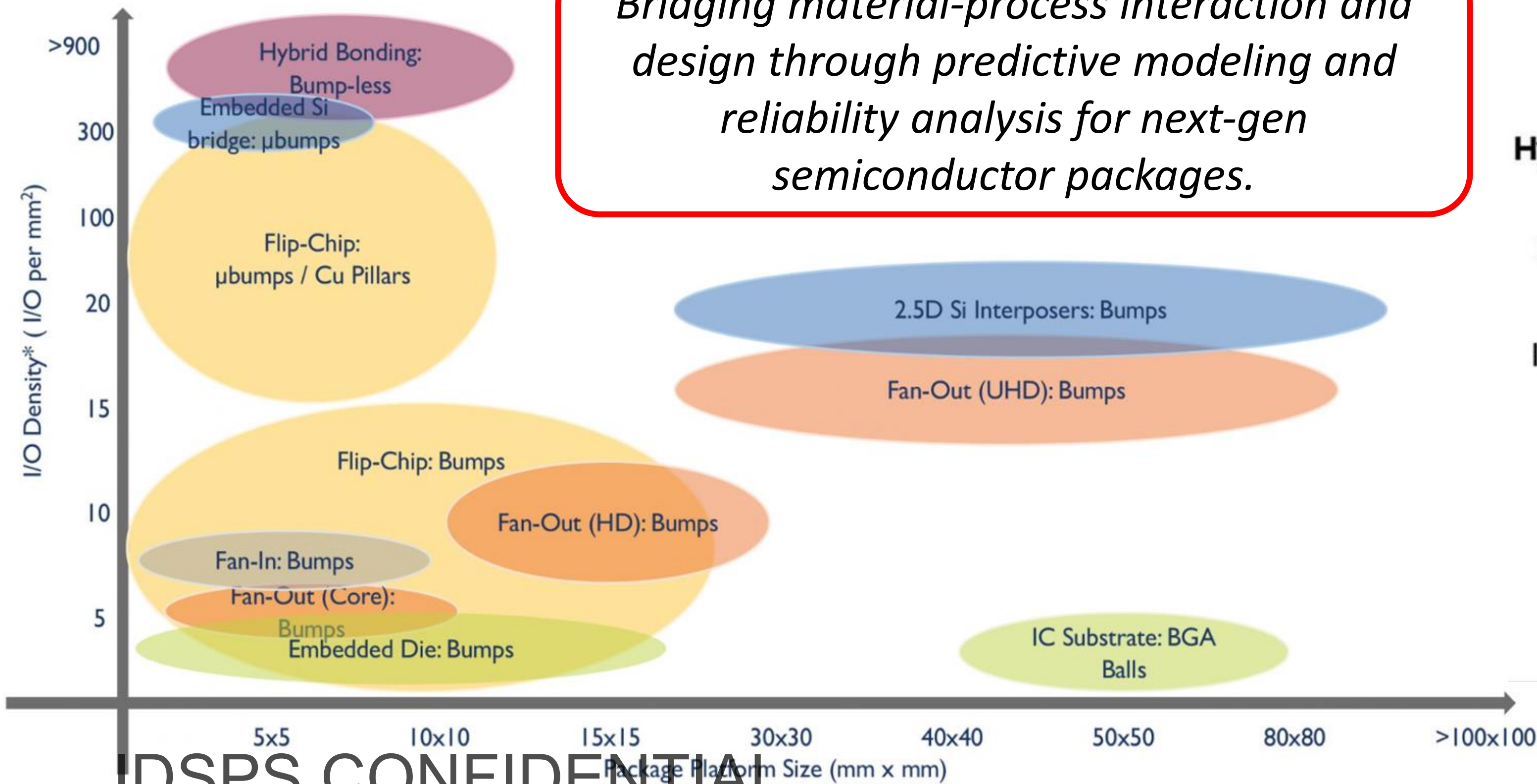


IDSPS CONFIDENTIAL

Next-Gen Industry Needs

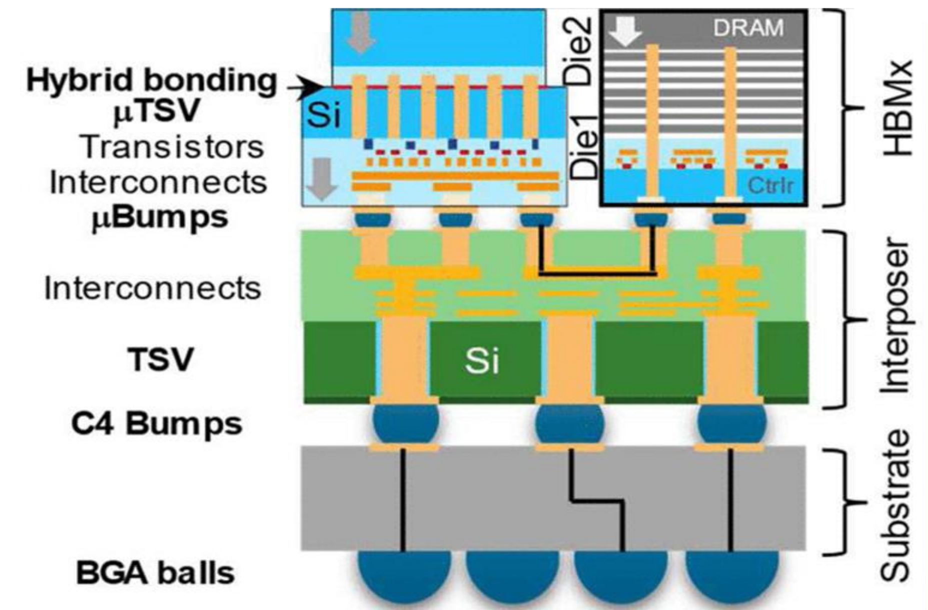
Heterogenous Integrated Systems promise **better performance, power efficiency, cost, and form factor** for HPC, AI, mobile, and automotive applications.

Bridging material-process interaction and design through predictive modeling and reliability analysis for next-gen semiconductor packages.



Source: Status of Advanced Packaging Industry 2020, Yole Development

An example of a complex Heterogeneously Integrated (HI) System



[X.-W. Lin, IEDM 2021]

IDSPS CONFIDENTIAL

Synopsys internal only

Challenges and roadmap for predictive modeling - semiconductors packaging & manufacturing

©2025 ANSYS, Inc. / Proprietary. Do Not Share.

Current Challenges

Semiconductor Manufacturing

1. **High fidelity simulations** to model complex, multi scale and multi-dimensional physics of manufacturing processes like solder reflow, wafer dicing, laser, CMP, etc. Currently R&D in this area is mostly in-house experience & experiments to come up with optimal process parameters
2. **Developing AIML techniques** to improve and enhance the fidelity & faster design cycles for manufacturing
3. **Develop best practises for Advanced processes** of manufacturing like Hybrid Bonding.

Semiconductor Design

1. **ECAD ←→ MCAD data conversions:**
   - **Streamlined standards and best practices to convert and utilize ECAD to MCAD data for Multiphysics simulations**
   - Ability to be able to share data and models with IP protection and Encryption across teams & vendors
2. **Solvers: With advanced ICs the model size is exploding:**
   - **Scalability of CAD and CAE Softwares to handle millions of** parts and >10's of millions of DOFs.
   - Advanced ICs are mainly driving this
3. **Data workflows and reuse**
   - Connecting 1D, 2D and 3D models as appropriate to fasten simulations as needed

Solder reflow

Wafer Saw Dicing

Wafer Laser Dicing

Wafer Backgrinding

Chemical Mechanical Polishing (CMP)

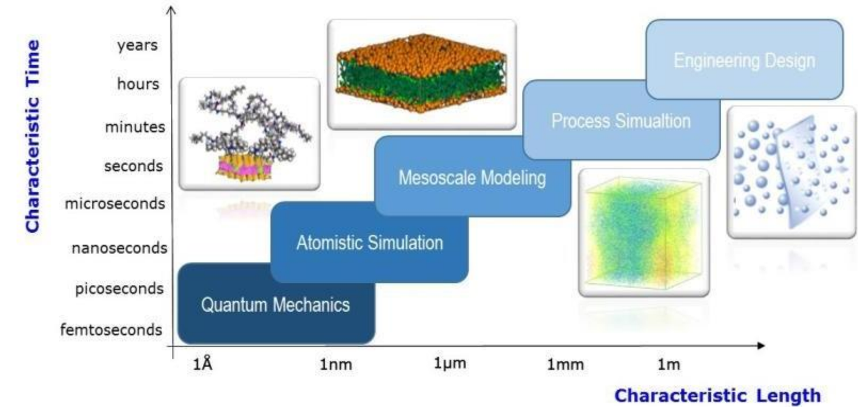
IDSPS CONFIDENTIAL

©2025 ANSYS, Inc. / Proprietary. Do Not Share.

Roadmap

Semiconductor Manufacturing

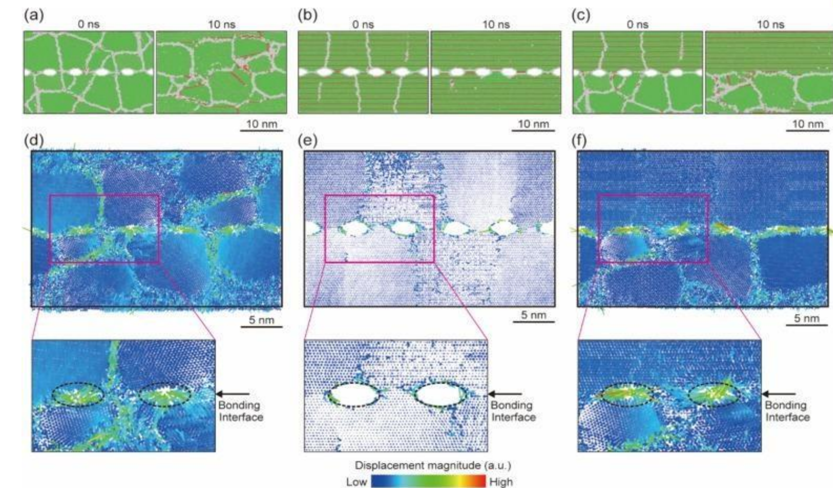
1. **AI for complex physics in Semiconductor Manufacturing:** More use of AI in scenarios which are difficult to solve using Mechanics principles.
2. **New Solver capabilities to** enable mesh-free, high-resolution modeling of electrical, fluid, thermal, and mechanical effects. Ideal for capturing complex geometry evolution and dynamic behaviors.
3. **Multiscale modeling**: Connects macro-scale process effects with micro-scale material responses.
4. **Atomic Scale model:** To capture the nanoscale behaviour essential for diffusion type of processes like hybrid bonding.
5. **Digital Twin:** Creates virtual replicas of manufacturing processes to test and optimize in-situ process.



https://www.molbnl.it/node/116

Semiconductor Design

1. **Automation**
   - To automate repetitive tasks
   - To eliminate the need for manual intervention wherever possible to streamline the workflow.
2. **High-Performance Computing (HPC) with GPU Acceleration:**
   - More scalable and GPU optimized solvers to run complex semiconductor simulations faster.
3. **Unified platform to consume Semiconductor files**
   - Need a unified platform that can manage different semiconductor and mechanical files to ensure consistency across tools.



https://www.sciencedirect.com/science/article/pii/S0264127524009511

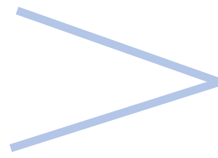
IDSPS CONFIDENTIAL

इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF
ELECTRONICS AND
INFORMATION TECHNOLOGY
©2025 ANSYS, Inc. / Proprietary. Do Not Share.

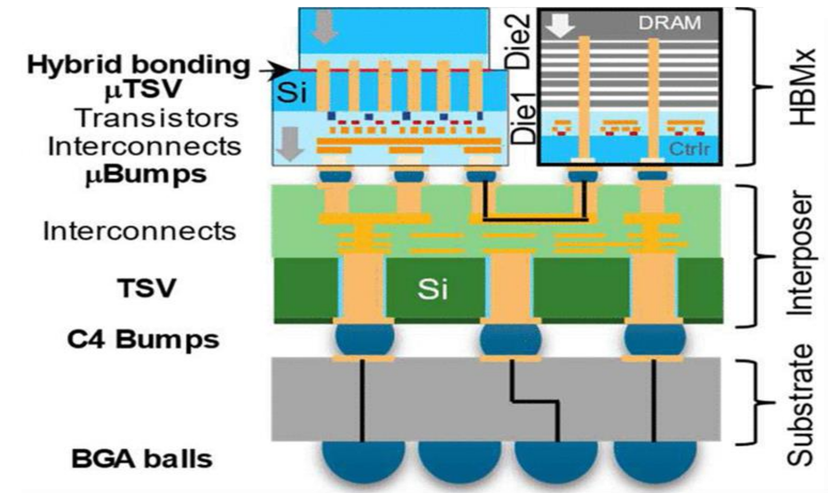
Ansys
part of Synopsys
इंडिया सेमीकंडक्टर मिशन
India Semiconductor Mission
Catalyzing India's Semiconductor Ecosystem
Indian DSPS R&D Team. Together, We Can.

Technical challenges in ensuring performance and reliability

- ❑ Chip-level
- ❑ Package-level
- ❑ System-level



Chip-Package Interaction (CPI)



[X.-W. Lin, IEDM 2021]

Chip	Electromigration	Crack propagation	Thermal stress in TSVs	BEOL dielectric breakdown	Solder/Cu-pillar bumps	HCI/BTI
Package	Warpage	Thermomechanical stress-induced failures	Interlayer delamination	Solder joint fatigue & brittle fracture		Moisture ingress
System	Failure mechanism identification & accelerated testing		Low-temperature Solder	Solder joint fatigue	Shock and Vibration reliability	Thermo-mechanical stress

IDSPS CONFIDENTIAL

Role of Predictive Modeling and Co-Design

To ensure the performance and reliability of a device/module and identify potential design risks ***before mass production***.

Electrical Simulation → Power and Signal Integrity

Joule heating and Temperature field

Thermal Simulations → Temperature Map and Flow Fields

Temperature Field

Mechanical Simulations → Shock and Vibration Analysis

Lifetime prediction

System level Reliability Analysis

ANSYS *SIwave*

ANSYS *Icepack*

ANSYS *Mechanical*

ANSYS *Sherlock*

IDSPS CONFIDENTIAL

Moving to a Multi-physics and Multi-Scale Modeling Paradigm

Predictive Modeling to inform the knowledge base for advanced packaging and heterogeneous integration

Device
Device Database
Device Design Flow
Analysis

Package
Package Database
Package Design Flow
Analysis

System
System Database
System Design Flow
Analysis

Current Modeling Flows

Device
Device Database
Device Design Flow

Package
Package Database
Package Design Flow

System
System Database
System Design Flow

Multi-physics models: Optical, Electrical, Thermal, Mechanical, etc

Multi-scale simulation: Co-simulation for performance & reliability

Processes/Metrology

Co-Design: Design workflow, data transfer, Global Optimization, Variability, Physical Design, DfX (Manufacture, Reliability, Test, etc.)

Source: HIR 2021 Roadmap, Modeling and SImulation

IDSPS CONFIDENTIAL

Modeling and Simulation Metrics

Metric	5 years	10 years	15 years
Development Time from Concept to Product	5 years	3 years	18 months
Accuracy of Material Model/Property	>50%	>75%	>90%
Accuracy of Modeling	>50%	>75%	>90%
Effectiveness of Modeling and Simulation	Validated modeling for known failure modes with multi-physics modeling at different levels	Accurate modeling for comprehensive failure modes/mechanisms, with combined multiphysics modeling with multiscale modeling	Accurate and predictive modeling for unknown failure modes/mechanisms, with comprehensive multiphysics modeling combined with multiscale modeling and stochastic modeling
Efficiency of Modeling and Simulation	Simulation tool capable of multiphysics modeling across different domains (chip/package/board/system) mainly based on linear analysis	Simulation tool capable of multiphysics and multiscale modeling across different domains with mixed linear/nonlinear analysis	Simulation tool capable of multiphysics and multiscale modeling across different domains with fully nonlinear analysis

IDSPS CONFIDENTIAL

Source: HIR 2021 Roadmap, Modeling and SImulation

Need for Material and Interface Characterization

Material composition

- *chemistry,*
- *structure,*
- *surface functionalisation,*
- *filler modality / properties & aspect ratio*

Material symmetry

- *anisotropy,*
- *inhomogeneity,*
- *gradients,*

Size

- *surface / volume ratio effects,*
- *nano-scale effects*
- *mean free path effects*

Process parameters

- *temperature,*
- *pressure,*
- *time*
- *media*

Loading parameters

- *temperature,*
- *moisture,*
- *time*

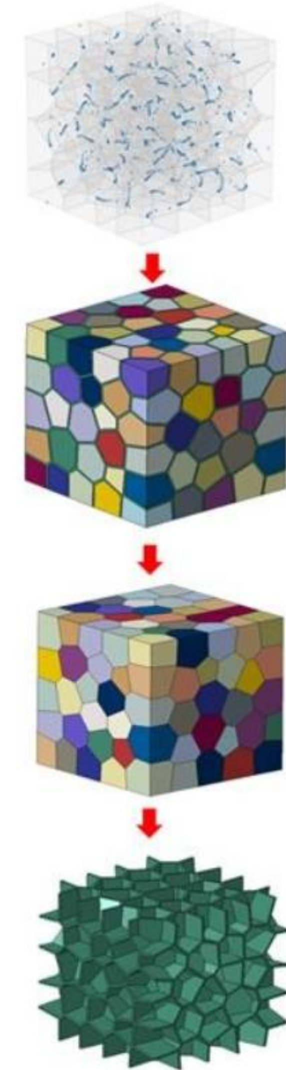
Load history → Mechanisms

- *fatigue damage, cracking,*
- *corrosion, migration*
- *degradation/ chemical aging,*
- *relaxation/ physical aging*

In response to all these influences, material properties can be

- linear or non-linear,

IDSPS CONFIDENTIAL



Ref.

Source: HIR 2021 Roadmap, Modeling and SImulation

Modeling Support to Other SRAs

Multi-physics and Multi-scale predictive modelling and design framework

Chip
Compute (Digital, Analog, Mixed Signal)
High Bandwidth Memory
Si, WBG (SiC, GaN)

Chip-Package-Board co-design
Physical design, global optimization, DfX

Multi-scale (Device-chip-package and package-board-system interactions)

Package
SiP, 3DIC, BGA, Flip-chip
WLP (Fan-in, Fan-out)
Interposers, TSV's
Solders, TIM, Wirebonds

Board/System
Organic, Ceramic etc.
Heterogeneous structures
Thermal management

Multi-physics (Thermal, Mechanical, Electrical and Chemical)

Multi-physics/scale Modeling
Scale: nm-um to cm-m

Market Applications
High-performance computing (HPC and Data centers)
High-power Automotive

Cross SRA support:

- Package Design
- Interconnecting Substrates
- IC & Board Assembly and Reliability
- System Design & Architecture
- Power Electronics

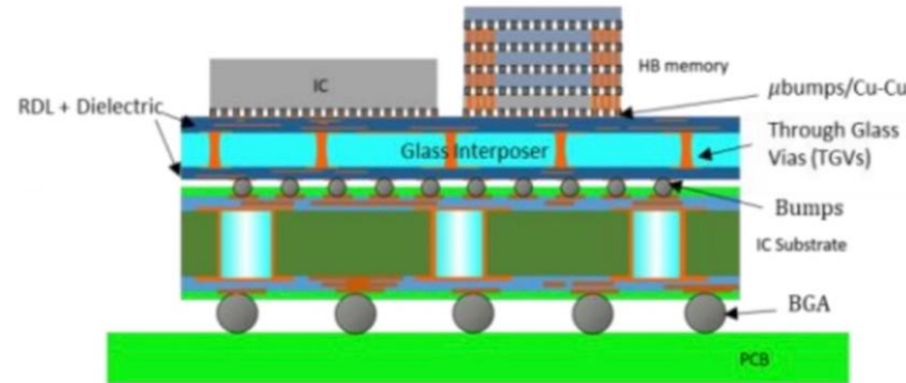
IDSPS CONFIDENTIAL

Strategic Focus Areas for R&D

AI assisted Design for Reliability and System Modeling
- Warpage
- Solder Joint Fatigue Life
- Electromigration risk prediction
- Thermal optimization of heterogeneous packages

- B. Rawat (IIT Ropar)
- S. Roy (IIT Kharagpur)
- A. Bhattacharya (IIT Kharagpur)

Next-generation high-performance computing module



Electrical/Electro-mechanical/Electro-thermal challenges
- Chip performance degradation due to TSVs
- BEOL and BSPDN integrity
- Thermal modeling for Cu-Cu hybrid bonding

- A. Bulusu (IIT Roorkee)
- T. Agarwal (IITGN)

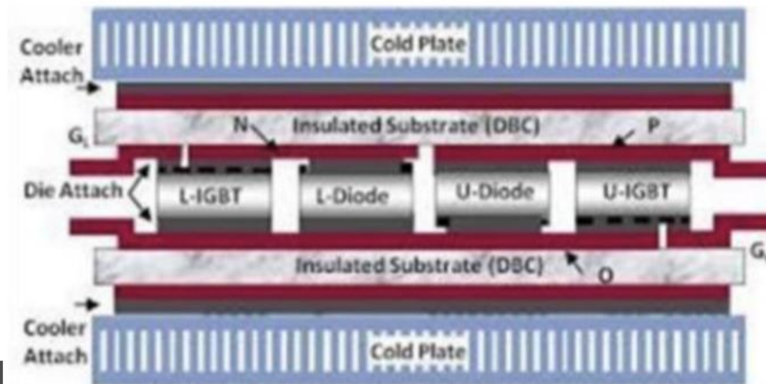
Thermo-mechanical challenges
- Package warpage
- Solder joint failure
- Shock and Vibration reliability

- R. Sastri Ayyagari (IITGN)
- D. Panchagade (FCRIT)

Material/Interface characterization for predictive models
- Novel materials for TIM
- Microstructure and strain mapping
- Low-temp. Solder joints

- P. Ghosh (IITGN)
- N. Sardana (IIT Ropar)
- N. Badwe (IIT Kanpur)

Next-generation high-power module



Creating Multi-physics platform
- RDL integrity (Polymer Dielectric Breakdown)
- CTE mismatch (polymer and Cu)
- Interfacial delamination

- V. KP Rao (BITS Pilani)
- D. Panchagade (FCRIT)

IDSPS CONFIDENTIAL

India-wide multidisciplinary Faculty with Expertise in the Strategic Areas

Core Faculty Team

Tarun Agarwal
(EE, IITGN) - Lead
First-principles multi-scale predictive modeling

Somnath Roy
(ME, IIT Kgp) - Co-lead
CFD (Heat flow), HPC & AI

Anand Bulusu
(ECE, IIT R)
System level modeling

Dhananjay Panchagade
(ME, FCRIT)
Failure oriented accelerated testing, Finite-element modeling

Ravi Sastri Ayyagari
(ME, IITGN)
Thermo-mechanical modeling of thin-films

Brajesh Rawat
(EE, IIT Ropar)
ML assisted reliability modeling

Pradipta Ghosh
(MSE, IITGN)
Microstructure characterization under Temp., strain

Neha Sardana
(MME, IIT Ropar)
2D material thin film growth

IDSPS CONFIDENTIAL

Cross-SRA Faculty with relevant expertise

Anandaroop Bhattacharya
(ME, IIT Kgp)
Thermal management

Nilesh Badwe
(MSE, IIT K)
Board Assembly

Shiladri Chakraborty
(EE, IIT B)
Power electronics, SiC pkgng.

Venkatesh KP Rao
(ME, BITS Pilani)
Multi-physics Finite Element modeling

Pradeep Dixit
(ME, IIT B)
Interconnects, Substrates

Rohit Sharma
(EE, IIT Ropar)
Package Design

Global partners and their expertise

US Faculty Collaborators

Prof. Abhijit Das Gupta, ME, University of Maryland, USA
-- Mechanics of electronic packaging materials and "smart" composite materials Research focused on nanomechanics, micromechanics, computational mechanics, damage mechanics and reliability physics

Prof. Ganesh Subbarayan, ME, Purdue University
-- Heterogeneous Integration and Advanced Electronics Packaging with a focus on thermomechanical behavior, reliability, and electrical-thermal-mechanical co-design

IDSPS CONFIDENTIAL

Research Project Proposals

- A Systematic Variability Aware Design Methodology for 3D ICs
  - PI: Anand Bulusu (IIT Roorkee)
- Multi-scale Electrical and Electro-thermal Modeling of Advanced Cu Interconnects and BSPDN
  - PI: Tarun Agarwal (IITGN)

Chip-package Interaction (Electrical performance and Electro-thermal reliability)

- Design and Multiphysics Modelling of Interfacial Failure Between Metal and Polymer Redistribution Layers of High-density Substrates
  - PI: Venkatesh KP Rao (BITS PILANI)

Multi-physics FEM

- Predicting Warpage in Compositionally Graded and Stacked Thin Films
  - PI: Ravi Sastri Ayyagari (IITGN)
- Damage Prediction of BGA board assemblies with SAC Solder interconnects exposed to Shock, vibration and extreme temperature environment
  - PI: Dhananjay Panchagade (FCRIT)

Predicting Thermo-mechanical reliability

- Reliability assessment of electronic packages with structure-property correlation
  - PI: Pradipta Ghosh (IITGN), Ravi Sastri Ayyagari (IITGN), Tarun Agarwal (IITGN)
- Investigating 2D materials based thermal interface materials (TIMs) for improved thermal management
  - PI: Neha Sardana (IIT Ropar), Tarun Agarwal (IITGN)

Material and interface thermal, mechanical characterization

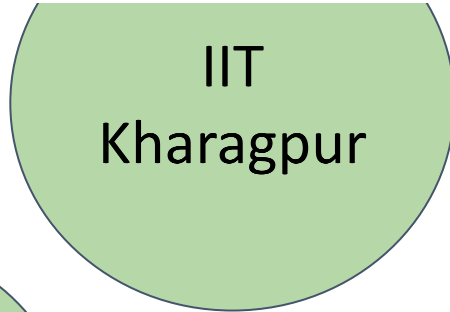
- ML Assisted Reliability Model for Electromigration Risk Prediction
  - PI: Brajesh Rawat (IIT Ropar)

AI assisted Design for Reliability

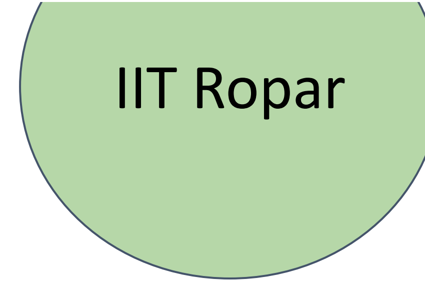
IDSPS CONFIDENTIAL

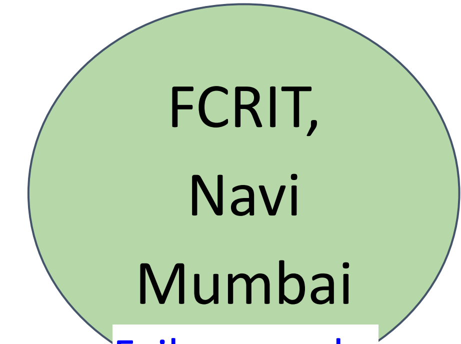
Hub and Spoke Research areas and institutions

Thermal design, Studying Heat Flow
AI assisted thermal modeling

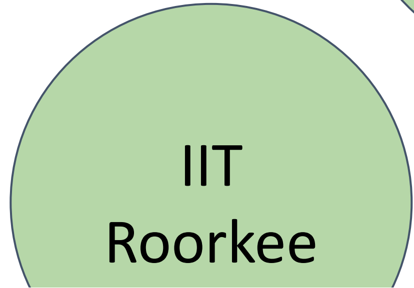


AI-assisted Reliability modelling
2D material based composites for TIM

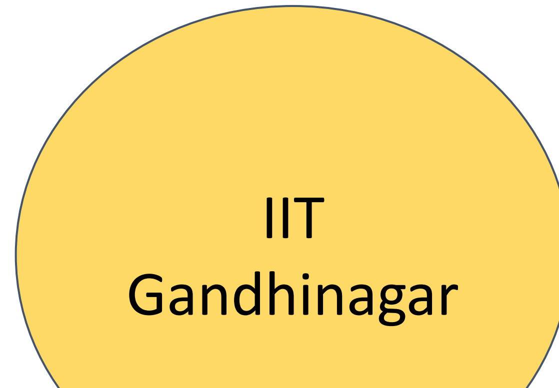




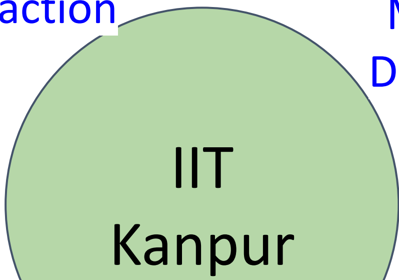
Failure mode accelerated testing



System level impact of chip-package interaction

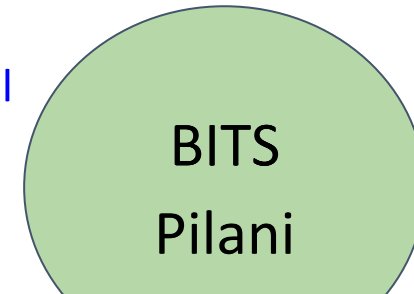


Material and Interface characterization
Multi-scale modelling for chip-package interaction
Developing Electro-thermal and thermo-mechanical numerical models



Material characterization of Board assembly constituents

IDSPS CONFIDENTIAL



Coupled Finite Element Solutions

Current and Potential Global and Indian Companies Interested in Research and Workforce

Currently Interested Industry Partners

Takatoshi Ikeuchi (Resonac)
Anil Kumar (Ansys)
Parthasarathy Ramaswamy (Intel)
Basant Saini Kaynes)
Gokul Kumar (Micron)
Taranjit Kukal (Cadence)
Texas Instruments
Globalfoundries
AMD
Applied Materials

Potential Future Industry Partners

Renesas
Tata Electronics
Siemens EDA
Invensas
ST Micro
Infineon

IDSPS CONFIDENTIAL

Technology Workforce educational programs

Introduction of Basic and Advance Courses in Curriculum

- Fundamental courses on "Chip/Package/Board-level Multi-physics Modeling" for UG students
- Bring currently offered graduate-level courses in semiconductor packaging to NPTEL platform
- **Educated workforce target (over 5(10) years) – B.Tech: 40 (200), M.Tech: 50 (90), Ph.D.: 10 (20)**
- Advanced courses on different aspects of predictive modelling and design for Senior UG, Masters and PhD students
- Lecture series from Industry Experts

Developing Hands-on Laboratories

- Labs equipped with necessary EDA, FEA tool licenses and Workstations, remote servers
- Package reliability testing facility development in the hub and spoke model
- Key experiments in different area of Reliability Modeling and Tests (Chip/Package/Board-level Coupled Electro-thermal, Electro-mechanical and Thermo-mechanical Simulations; Failure and Fatigue Tests (Electrical, HAST, Humidity Tests, Shock & Vibration Tests))

Specific (Certification) Courses for Industry Engineers

- Develop certification courses according to Industry Needs in the areas of Package Reliability Modeling and Testing

IDSPS CONFIDENTIAL

A Systematic Variability Aware Design Methodology for 3D ICs

PI: Anand Bulusu (IITR)

Objective - Development of a design methodology for circuits, initially buffers and level shifters, placed close to a through-silicon via (TSV)

Prior Art

- ❑ Current design methods depend on increasing margins (e.g., KOZ) to mitigate significant mechanical stress and temperature fluctuations near TSVs, leading to high area usage.
- ❑ Prior studies on buffer placement near TSVs to minimize delay, often relying on simplistic assumptions.
- ❑ Existing vendor tools claim an integration of temperature
- ❑ Doesn’t offer design and mechanical stress considerations in 3D-IC simulations.
  - ❑ Requirement of a large SPICE simulation time after every design iteration methodology.

IDSPS CONFIDENTIAL

Proposed Approach

- ❑ Buffer design methodology considering TSV in a 3D path.
- ❑ Timing Models for circuits placed near a TSV.
- ❑ Inclusion of thermo-mechanical effects due to TSV in design of circuits placed near a TSV.
- ❑ Inclusion of aging effects of TSV and devices placed in the vicinity of TSV.
- ❑ Development of methodology/tool for design of driving and receiving circuits for signals passing through TSV.

Outcome and Impact - A Python-based tool is proposed for optimal buffer design and insertion methodology in a 3D logic/clock path based on user’s requirement, thereby ensuring timing performance.

Electro-thermal analysis and optimization of nTSVs in BSPDN

PI: Tarun Agarwal (IITGN)

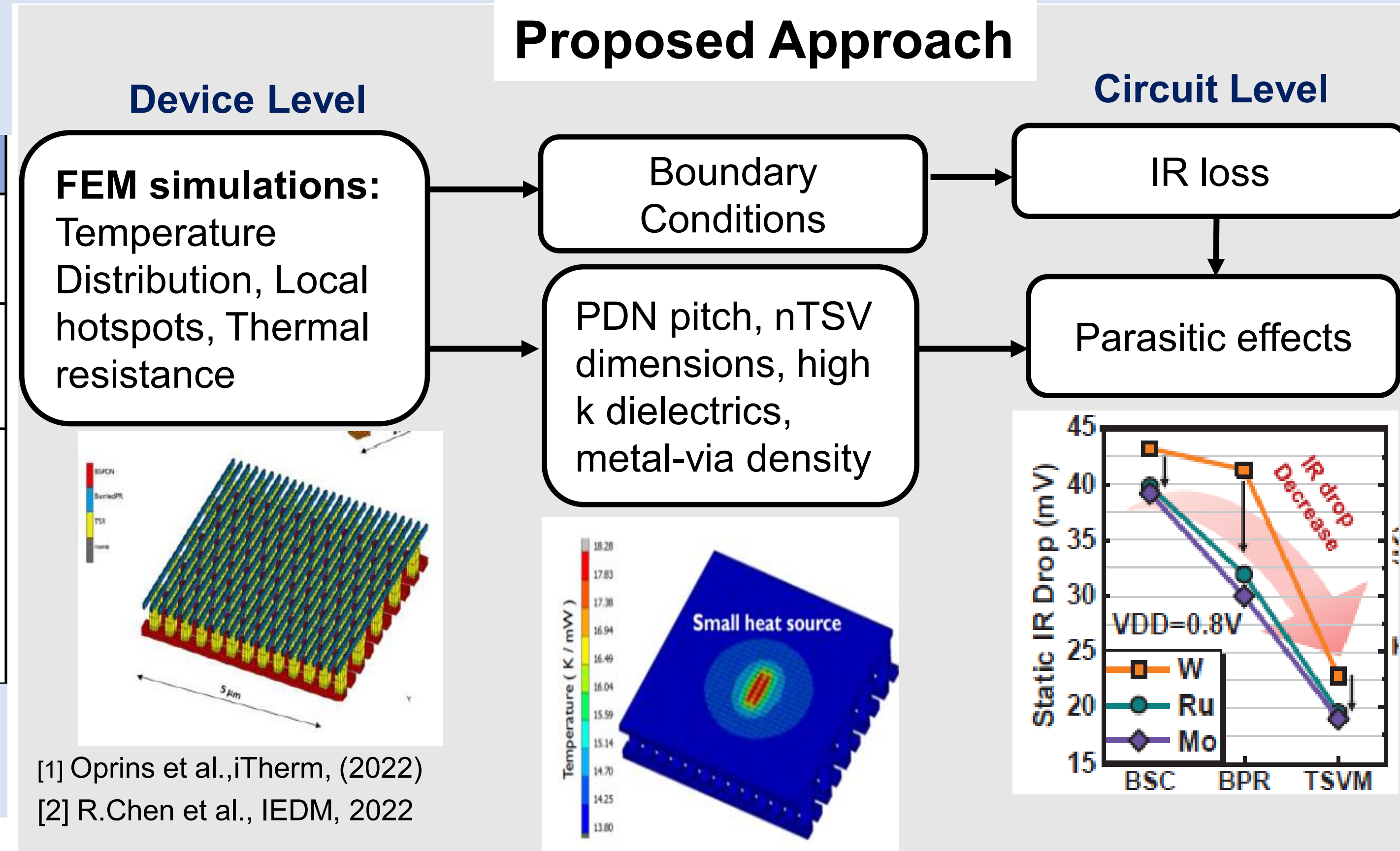
Objective - Develop a framework combining electrical-thermal analysis at device and circuit level to achieve an optimized BSPDN structure

Industry Need – Reduced self heating in BSPDN and optimized nTSV.

Key Components	Prior Art	Proposed
Electro-thermal	Yes	Yes
FEM analysis with high-κ dielectrics	No	Yes
IR drop and hotspot co-optimization with alt barriers and dielectrics in BSPDN network	No	Yes

Outcome– Multi-scale framework to optimize nTSV interconnects in BSPDN.

IDSPS CONFIDENTIAL



Design and Multiphysics Modelling of Interfacial Failure Between Metal and Polymer Redistribution Layers of High-density Substrates

PI: Venkatesh KP Rao (BITS PILANI)

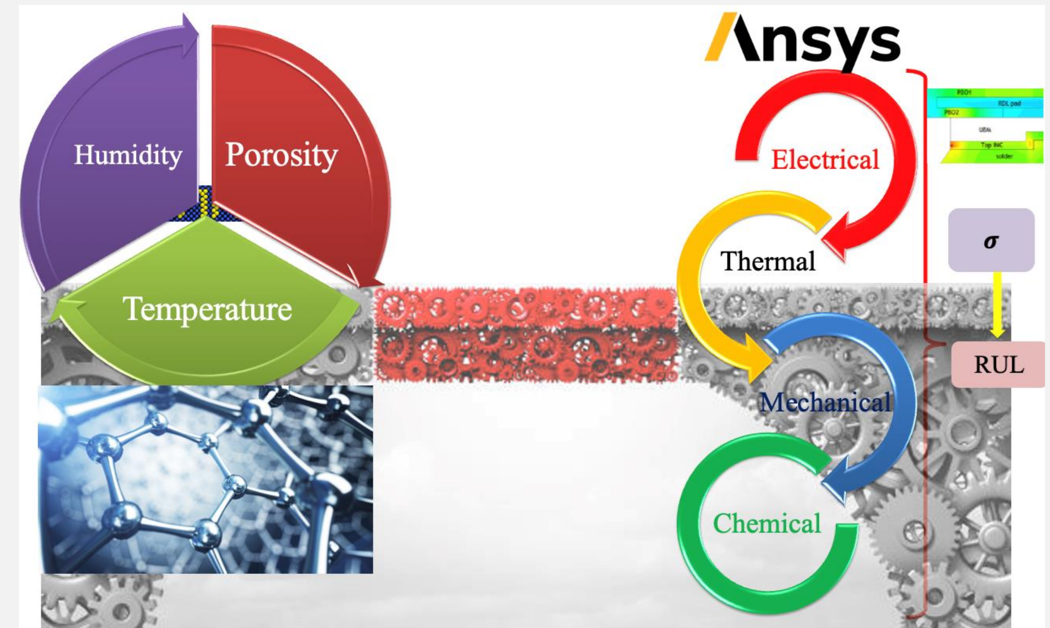
Objective - Develop Multiphysics platform, which involves the electrical, chemical, thermal, and mechanical physics to study the failure mechanisms in RDLs.

Parameter	Prior Art	Proposed
Physics handled	Only two physics were coupled	Electrical, chemical, thermal and mechanical physics are not explored
Effect of chemical treatment	Not considered	The effect of chemical treatment on mechanical response is will be taken into account
Bridging gap between continuum and molecular regime	Not considered	Gap will be bridged

Salunke, Ashish S., et al. (2023).
Shahmardani, M., Mohammadi, R. (2022).
Hirsch, Franz, Erik Natkowski, and Markus Kästner. (2021)

IDSPS CONFIDENTIAL

Proposed Approach



Predicting Warpage in Compositionally Graded and Stacked Thin Films

PI: Ravi Sastri Ayyagari (IITGN)

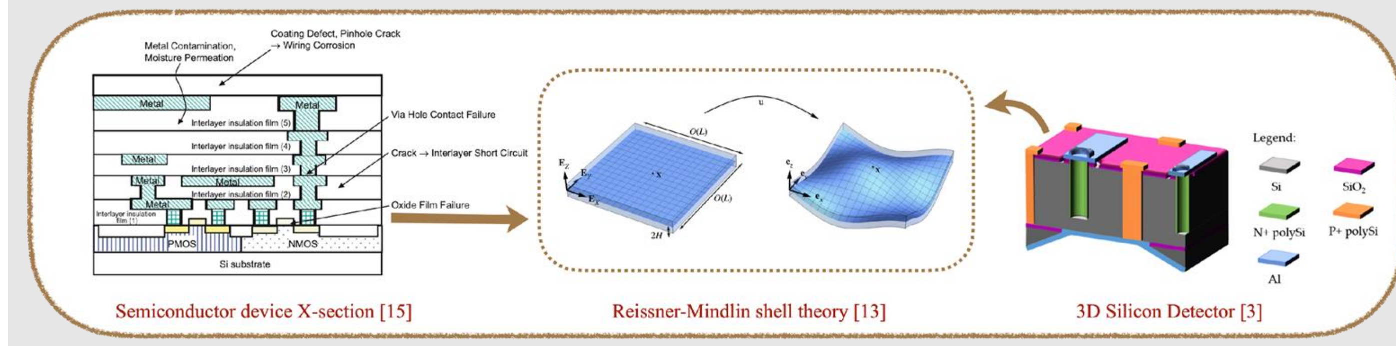
Objective - Aims to provide **design guidelines to effectively counter warpage** (large out-of-plane deflections) and **elastic instabilities** (buckling and local curvature changes) in thin films

Key Components	Prior Art	Proposed
Finite Deformation Theory	Yes	Yes
Thermo-Mechanical Coupling	Yes	Yes
Smoothed and Enriched Finite Elements	Enriched FE Only	Yes
Compositionally Graded Configurations	No	Yes
Heterogeneous Stacking	Elastic Only	Elastic and Hyperelastic

IDSPS CONFIDENTIAL

Proposed Approach

- Develop a Hyperelastic thermo-mechanical Reissner-Mindlin shell theory with layups handled using HSDT and smooth & Enriched FE.
- Films with variation in elastic properties, mismatch strains through thickness, in-plane strain gradients and anisotropy will be considered.



Semiconductor device X-section [15]   Reissner-Mindlin shell theory [13]   3D Silicon Detector [3]

H-C Cheng et al., *Materials* **2021**, *14*(17), 4816.
W. Yu et al., Computer Methods in Applied Mechanics and Engineering **2002**, 191(44), 5087-5109.

Damage Prediction of BGA board assemblies with SAC Solder interconnects exposed to Shock, vibration and extreme temperature environment

PI: Dhananjay Panchagade (FCRIT)

Objective - Prediction of material and interface failure for damage equivalency and development of failure envelopes for BGAs. Assessment of design margins at solder copper, solder-intermetallic, copper organic laminate.

Key Components	Prior Art	Proposed
High strain-rate material properties	No	Yes
Shock/Vibration/ Thermal aging overlap	Yes	Yes
Thermal Cycling ramp rate	No	Yes

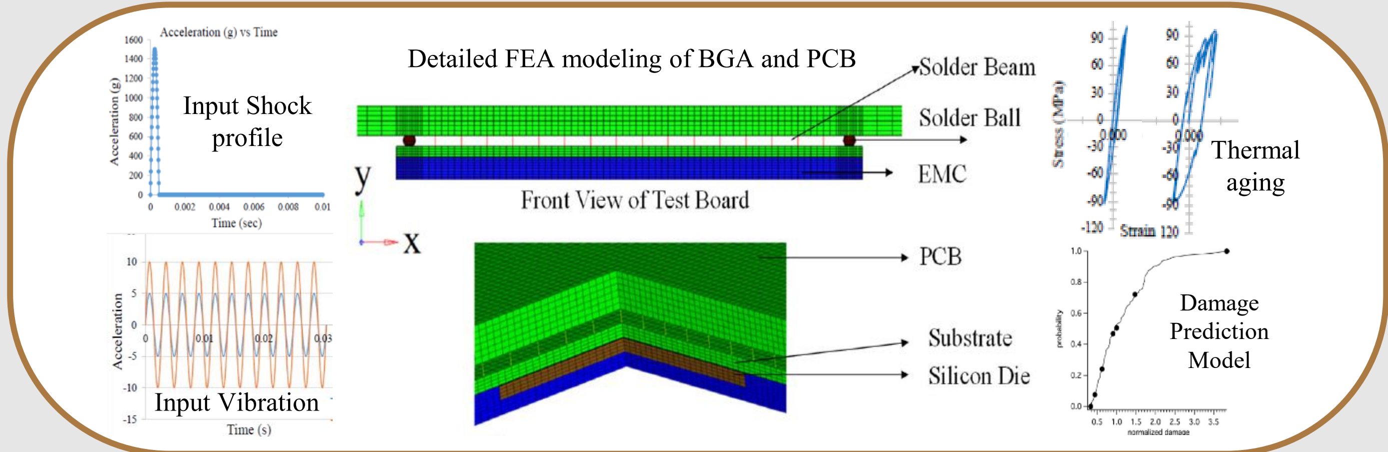
Outcome – Damage Prediction model incorporating Shock, vibration and temperature aging.

[Industry: Aviation and Defense]

IDSPS CONFIDENTIAL

Proposed Approach

- Develop overlapping shock. Vibration and temperature model.
- Use high strain-rate material properties for shock and drop model.
- Study the effects of ramp rates for thermal cycling in the FE model.



Reliability assessment of electronic packages with structure-property correlation

PI: Pradipta Ghosh (IITGN)

Objective - Quantification of strain fields and induced defects in electronic packages during thermal cycling to develop failure models for predictive modelling

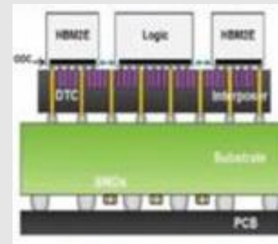
Key Components	Prior Art	Proposed
Finite Element Simulation	Yes	Yes
Thermo-Mechanical Coupling	Yes	Yes
Verification of model with experiments	Partially	Yes
Experimental quantification of defects	Yes	Yes
Correlation of measured microstructure, strain and defects for failure models	No	Yes

Outcome – Microstructure and strain based models for Predictive modeling framework.

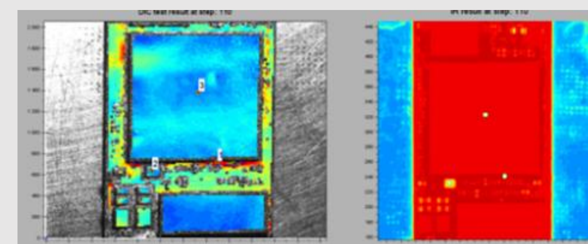
IDSPS CONFIDENTIAL

Proposed Approach

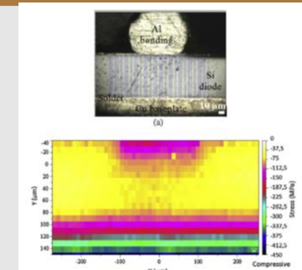
- ❑ Use model package geometries with various components for experimental quantification of strain using Optical/Laser/Raman based techniques.
- ❑ Extensive radiography and microscopy to identify the defect kinetics.



3D Architecture



Optical and IR based strain-Temperature



Raman strain mapping

[1] Kociniewski et al., "μ Raman spectroscopy for stress analysis in high power silicon device", Microelectronic Reliability 2014
[2] Dantec Dynamics

Investigating 2D materials based thermal interface materials (TIMs) for improved thermal management

PI: Neha Sardana (IIT Ropar), Tarun Agarwal (IITGN)

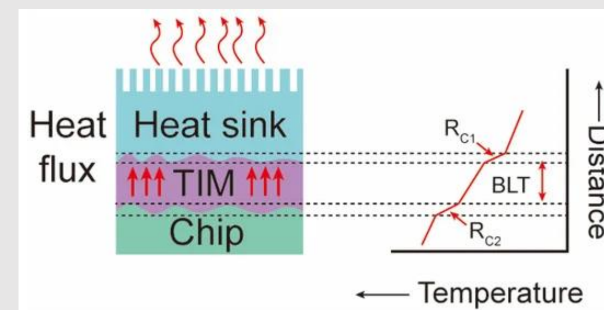
Objective - Aims to provide **design guidelines to improve heat dissipation efficiency** in high-power modules.

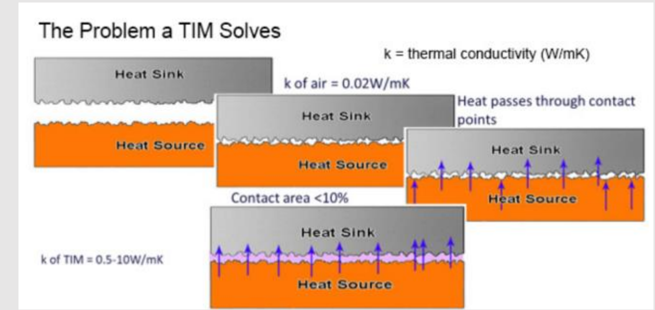
Key Components	Prior Art	Proposed
Effect of multi-layer graphene film thickness	Yes	Yes
Atomistic investigation of interfacial layer between TIM and Si	No	Yes
Investigating role of filler material in 2D TIMs	Yes	Yes

IDSPS CONFIDENTIAL

Proposed Approach

- Atomistic Investigation for 2D materials based TIMs
- Material characterization of 2D TIMs with filler materials
- Films with low interfacial thermal resistance, high thermal conductivity, easily deformed by contact pressure will be considered.





Zheng, W., Shao, C., Wang, Q., Li, G. and Li, H., *Surfaces and Interfaces*, 2023

Xing, W., Xu, Y., Song, C. and Deng, T., *Nanomaterials*, *12*(19), 2022.

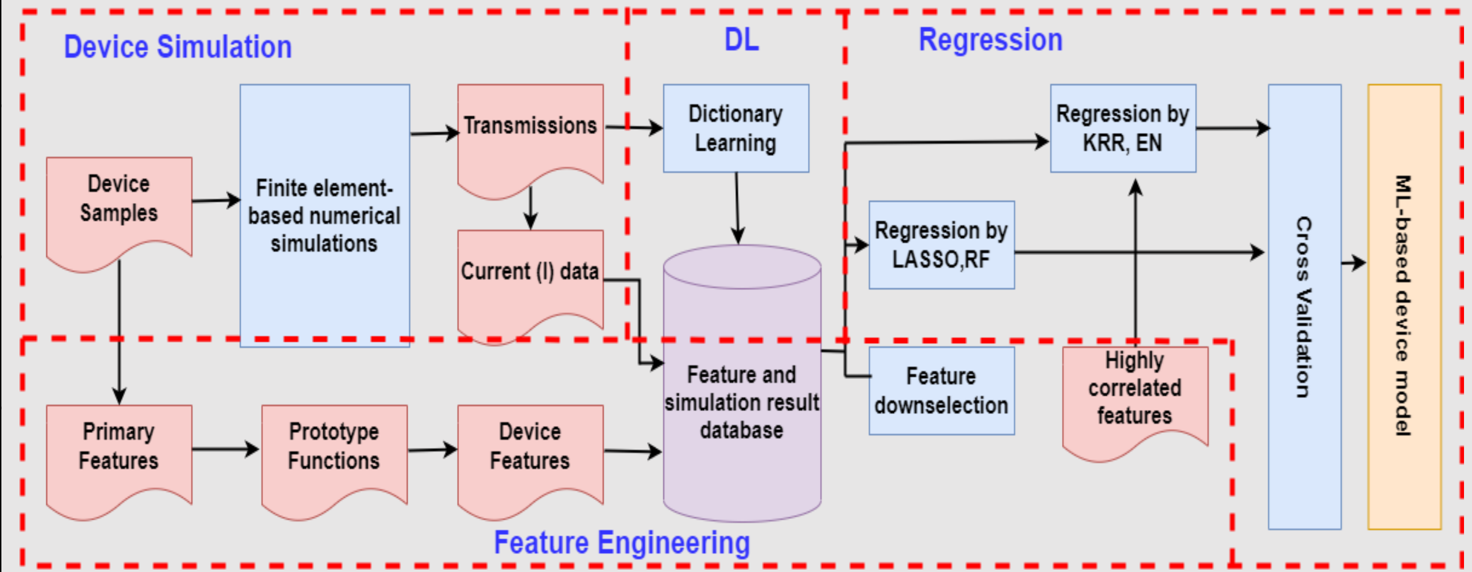
ML Assisted Reliability Model for Electromigration Risk Prediction

PI: Brajesh Rawat

Objective - Apply machine learning framework to co-design the interconnect and power module for mitigating electromigration challenges

Modeling approaches	Prior Art	Proposed
ML- algorithm in conventional FEM loop [1]	Yes	Yes
First principles study of emerging materials [2]	Yes	Yes
First principles + Microstructure + FEM modeling [3]	Yes	Yes
Material Predictions from space for EM Risk Minimization using ML-technique	No	Yes

Proposed Approach



Outcome – ML based electromigration predictive model for given trace layout

IDSPS CONFIDENTIAL

[1] Zho et al. Micromachines 2022
[2] Chang, Chao et al., Journal of Materials Research and Technology, (2022)
[3] Mukesh S et al. ,IEEE Transactions on Electron Devices, (2023).

Facilities required

- Bridging material-process interaction and design through predictive modeling for next-gen semiconductor packages.

Basic Package Assembly Equipment (~ 10 CR)

1. Manual Wafer prober
2. Backgrinding
3. Dicing Saw
4. Wafer mount, UV cure
5. Die attach, Die bonder, Underfill dispense
6. Wirebond
7. Reflow oven

Basic characterization (~8 CR)

1. Shear/Pull tester
2. X-ray
3. CSAM
4. TMA/DMA
5. High mag. Microscope

Reliability Testing (~ 7 CR)

1. Nanoindenter (with thermal stage)
2. Digital Image Correlation (DIC) system for warpage
3. Temperature Cycling Chamber
4. THB / HAST Chamber
5. High-Resolution DAQ System

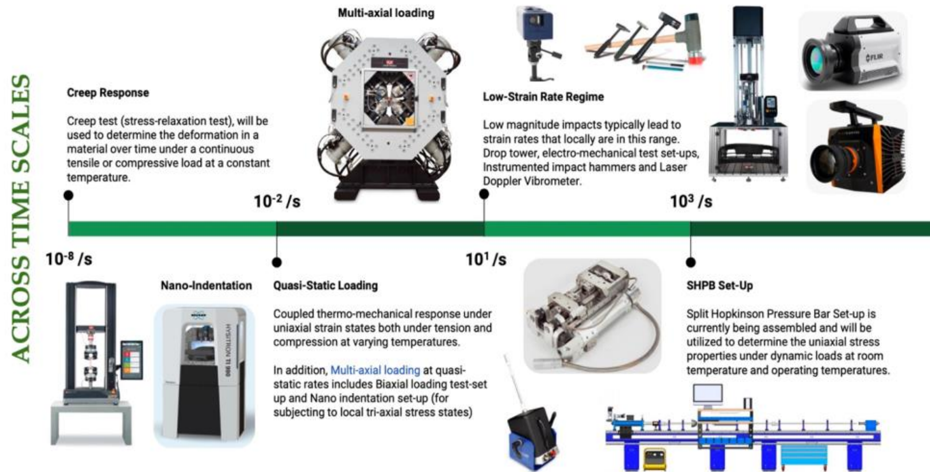
Predictive Modeling Infrastructure (~ 4 CR)

1. HPC Clusters
2. FEA Tool licenses (ANSYS, COMSOL)

IDSPS CONFIDENTIAL

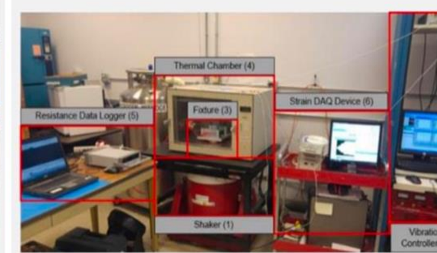
Characterization Facilities

Mechanical Characterization lab



Failure mode stress tests lab

Thermal cycling chamber

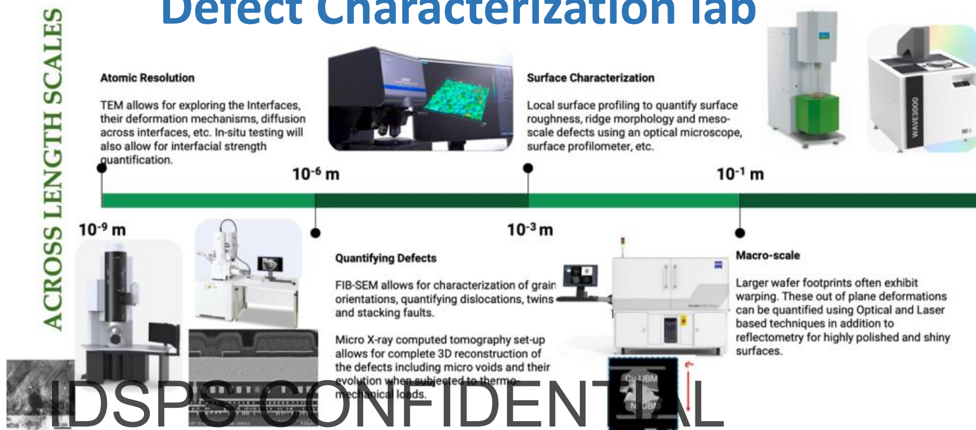


Temperature - Humidity - Vibration Chamber

High Accelerated Life Test with shock vibration

Data Acquisition System

Defect Characterization lab



IDSPS CONFIDENTIAL

Thermal Characterization lab

Infrastructure required

- ❑ FEA Multi-physics and EDA Tool licenses (Existing at IITGN)
- ❑ High performance clusters + Workstations (Existing at IITGN)

Materials Metrology and Reliability Test for Model Development/Calibration:

- ❑ Environmental controlled furnace
- ❑ Spatially resolved micro-Raman spectroscopy
- ❑ High temperature nano-indenter
- ❑ Thermo-mechanical fatigue with digital image
- ❑ HAST Highly Accelerated Stress Test Chamber, Thermal cycler
- ❑ Temperature and Humidity Chamber
- ❑ Dynamic Mechanical Analyzer
- ❑ Temperature Vibration Chamber
- ❑ Automatic Package Testers
- ❑ Cyclic Mechanical Loader
- ❑ Shock and Vibration tables and platforms
- ❑ Warpage measurement metrology
- ❑ Thermal Imaging cameras and optical microscope

IDSPS CONFIDENTIAL

Five-year Milestones

Deliverables	Year 1	Year 2	Year 3	Year 4	Year 5
Formation of SRA Consortium with industry members					
Definition of projects					
Set up primary research CoEs –Spoke and Hubs					
Set up infrastructure					
Develop Educational Programs					
Project Goals Review					
PMD for indigenous designs (Cross SRA)					
Educate ~ 40 graduate students (M.Tech. and Ph.D.) across the country, UG specialization running					
Execution of new project proposals					

IDSPS CONFIDENTIAL

Thank You

IDSPS CONFIDENTIAL