Next-gen Advanced Materials (Packaging and Beyond-CMOS Devices)

Industry Co-Development Center (ICC) with Industry Consortium for Next Gen Research and Workforce

Bhagwati Prasad, IISc Bengaluru (Lead)
Praveen Kumar, IISc Bangalore (Co-Lead)
Murali K P, NITC (Co-Lead)

&

Ravi Bhatkal, MacDermid Alpha, India (Industry Lead)
Arun Chandrasekhar, Intel India (Industry Co-Lead)

Global Academic Collaborators

Prof. Raj Pulugurtha (FIU) – Packaging Materials
Prof. R Ramesh (Rice University) – Beyond CMOS Memory Materials

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Materials are the Backbone of All Technologies

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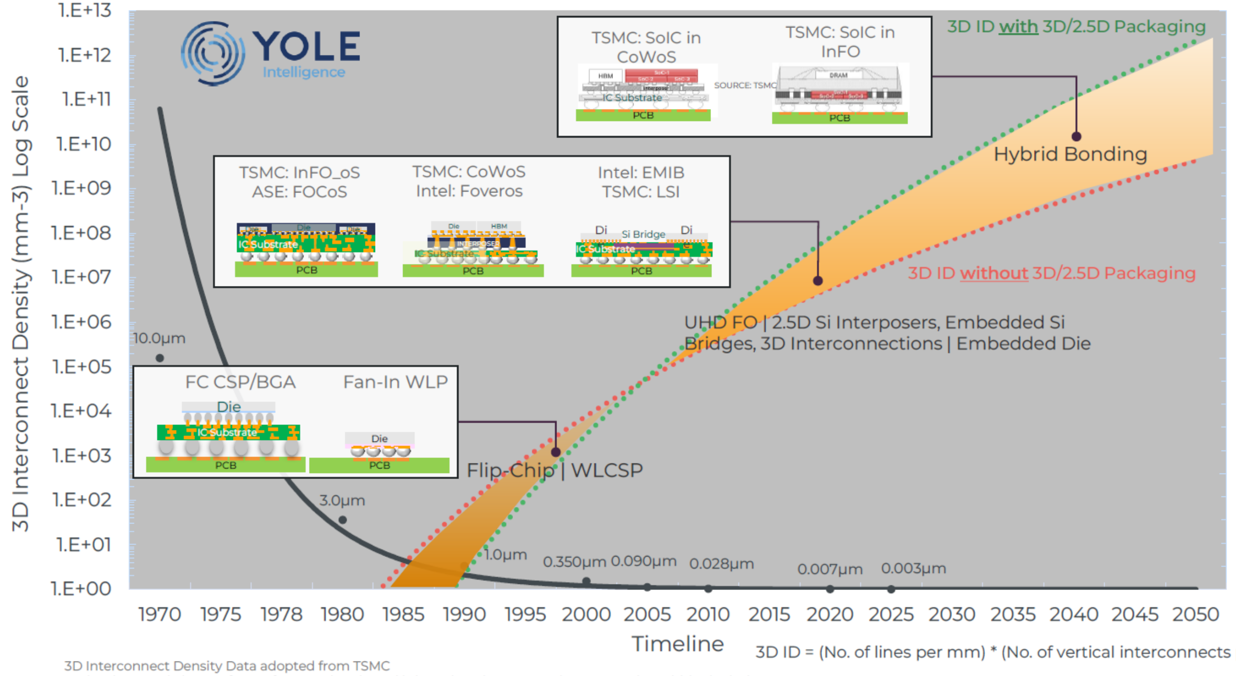
Packaging Materials: Next-Gen Industry Needs and Technical Challenges

High-end Performance Packaging And Hetero-integration: Require Novel Materials and Process Innovations

SEMICONDUCTOR PACKAGING ROADMAP

Combined Timeline of 3D Interconnect Density & Technology Node



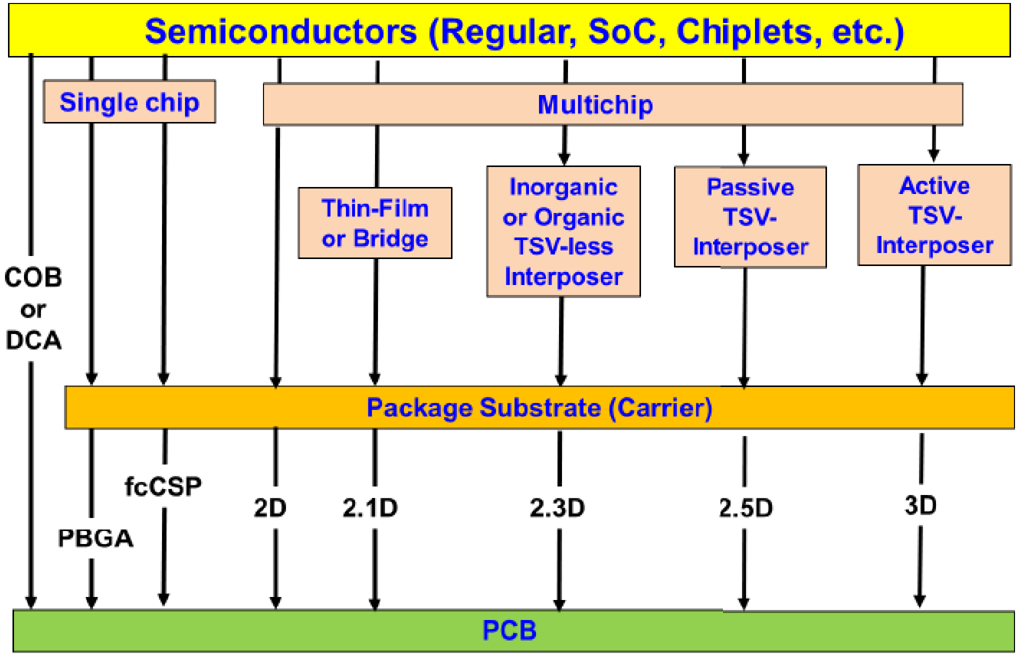
3D ID = (No. of lines per mm) * (No. of vertical interconnects per mm^2)

3D Interconnect Density Data adopted from TSMC

Technology Node here refers to front-end node and is based on the expected average value within the industry.

YOLE Intelligence

Technology & Market Trends for Advanced Packaging | SSI 2023 | www.yolegroup.com | ©



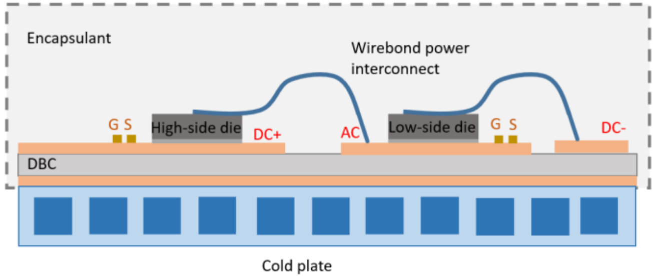
IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY, VOL. 12, NO. 2, FEBRUARY 2022

Packaging Materials: Research Vision (Current vs. Proposed)

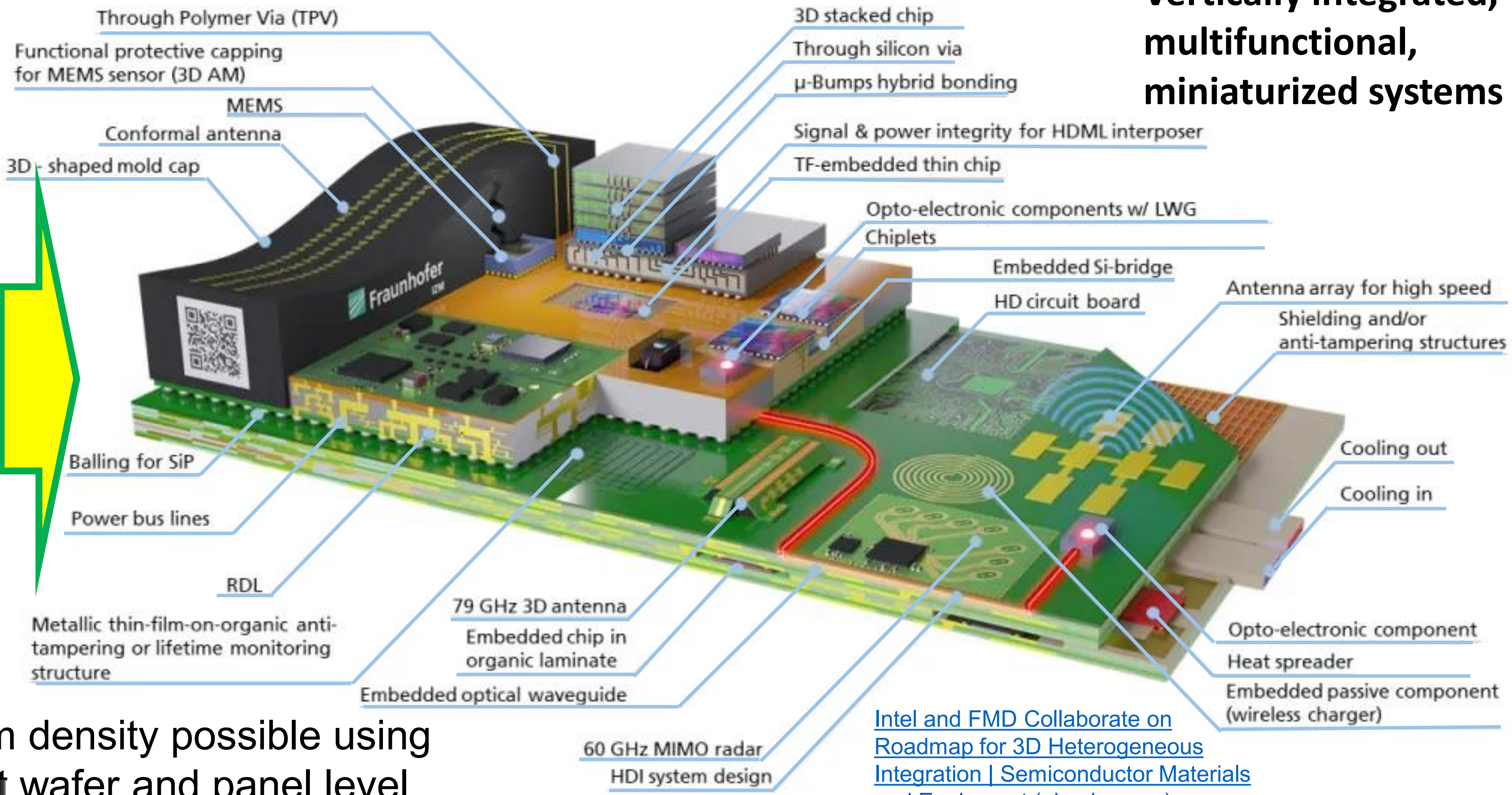
(Proposed) - **Wire-bondless, heterogeneously-integrated 3D**

- Large footprint
- High parasitics
- Limited integration density
- Thermal bottlenecks

(Current) - **Single-side-cooled, wire-bonded, soldered, 2D**



Vertically integrated, multifunctional, miniaturized systems



[Intel and FMD Collaborate on Roadmap for 3D Heterogeneous Integration | Semiconductor Materials and Equipment (abachy.com)]

The highest electronic system density possible using heterogeneous integration at wafer and panel level

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Materials (Packaging and Beyond-CMOS Devices)

Key Objectives

- **Develop Packaging Materials for Other ICCs:** Consult with other ICCs to identify critical areas for development
- **Set Up Infrastructure for R&D and Education:** Aim to train over 1000 personnel in semiconductor packaging and device materials processes within five years
- **Define Industry Projects with Global Companies:** Identify companies within this SRA to form an R&D consortium
- **Develop Novel Packaging Materials for Next-Generation Technologies – For Power components, High frequency dielectric, and EMI shielding**
- **Advanced Quantum Materials for Quantum Computing, Quantum Communication, and Quantum Sensing, and their Packaging**
- **Develop Novel Packaging and Device Materials for Extreme Environments (high/low temperatures, space, high radiations, high pressure, etc.):** Focus on applications essential for national security and strategic needs
- **Develop Functional Materials for Beyond-CMOS Computing:** Target advancements in AI, IoT, sensors, non-volatile memory, and emerging data storage and AR/VR applications

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Materials (Packaging and Beyond-CMOS Devices)

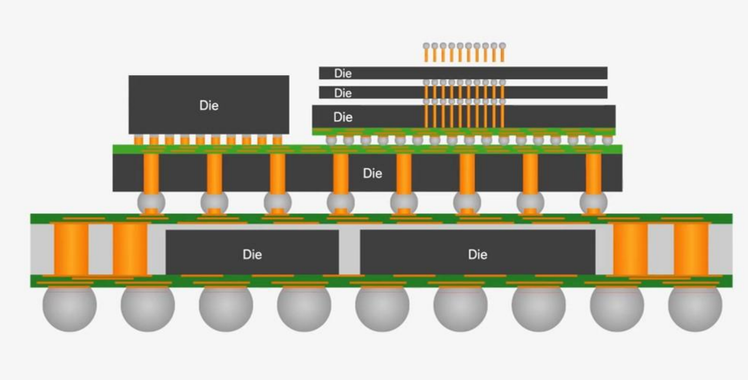
Interconnecting Substrates

Co-Packaged Optics

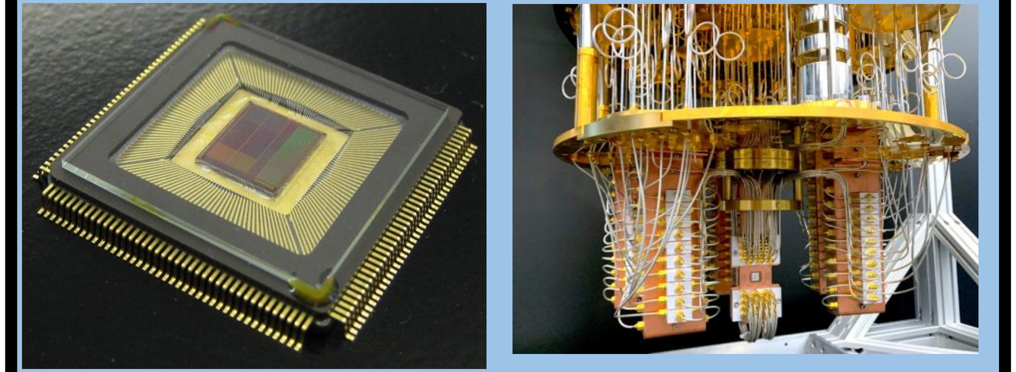
6G Integrated Systems

Integrated Sensors & MEMS

Quantum technology



Materials – Packaging Materials



Materials – Beyond CMOS Devices Materials

Thermal Management

Power Electronics

IC & Board Assembly and Reliability

Emerging Memory Devices

Materials for AI and Neuromorphic Chips

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Packaging Materials: Research Vision (Current vs. Proposed)

Category	Current Materials	Proposed Materials	Expertise in Proposed Mat. Devlp.
❖ **Encapsulation/Molding Compounds**	- Epoxy-based molding compounds - Thermosetting resins - Silicones (high thermal stability)	- Bio-based epoxy resins - Low-stress molding compounds - Graphene-infused resins - Nanocomposite encapsulation for extreme environments	**Praveen Ramamurthy** (MTE, IISc) **Deepak Arora** (CE, IIT J)
❖ **Die Attach Materials**	- Silver-filled epoxies - Solder pastes (tin-lead, SAC alloys) - Organic adhesives	- Nano-silver pastes - Sintered materials - Conductive polymers with graphene - Hybrid bonding materials for 3D stacking	**Shiv Govind Singh** (EE, IIT H) **Suryasarathi Bose** (MTE, IISc)
❖ **Substrates**	- FR-4 (fiberglass-reinforced epoxy resin) - BT resin - Polyimide substrates - Copper-clad laminates	- Glass interposers - Flexible organic substrates - Fan-out wafer-level packaging (FOWLP) substrates - Low-temperature co-fired ceramic (LTCC) with integrated components	**Pradeep Dixit** (ME, IIT B) **Subho Dasgupta** (MTE, IISc)
❖ **Lead Frames**	- Copper (Cu), copper alloys - Alloy 42 (Nickel-iron alloy) - Silver or tin plating	- Thin-film metal composites - Organic lead frames - Nanomaterial-enhanced lead frames - Conductive polymer alternatives	**Deepak Arora** (CE, IIT J) **Suryasarathi Bose** (MTE, IISc)
❖ **Underfill Materials**	- Epoxy-based underfill - Thermally conductive underfills - Capillary and no-flow underfills	- Nanofiller-infused underfills - Reworkable underfills - Self-healing underfills - High-temperature stable underfills for wide-bandgap semiconductors	**Madhusudan Singh** (EEE, IIT Delhi) **Ankush Bag** (EE, IIT G)
❖ **Thermal Interface Materials (TIM)**	- Thermal greases - Phase change materials (PCMs) - Thermally conductive adhesives	- Graphene-based thermal pads - Carbon nanotube TIMs - Liquid metal TIMs - Hybrid organic-inorganic TIMs for 6G systems	**Anandaroop Bhattacharya** (ME, IIT Kgp) **Praveen Ramamurthy** (MTE, IISc)
❖ **Wire Bonding Materials**	- Gold (Au) wire - Copper (Cu) wire - Silver alloy wires	- Nano-gold/nano-copper wires - Aluminum-nitride composite wires - Carbon nanotube wire bonding - 2D materials (graphene, MoS_2) for 6G and ultra-thin interconnects	**Praveen Kumar** (MTE, IISc) **Nilesh Badwe** (MsE, IIT K)
❖ **Co-Packaged Optics (CPO)**	- Silica glass fiber - Polymer waveguides - Photonic ICs	- Silicon photonics - Hybrid organic-inorganic photonic materials - Plasmonic materials - Quantum dot-based materials	**Naresh Emani** (EE, IIT H) **Madhusudan Singh** (EEE, IIT Delhi)
❖ **6G Materials (High-Frequency)**	- GaAs (Gallium Arsenide) - InP (Indium Phosphide) - SiGe (Silicon-Germanium)	- Wide-bandgap semiconductors (GaN, SiC) - 2D materials (graphene, MoS_2) - High-frequency dielectric materials - Metamaterials for RF and compact antenna design	**Parlapalli V Satyam & Akshay K (EE, IIT Bhub.)** **Ankush Bag (EE, IIT G)** **Murali K P, Yogesh N (NIT Calicut)**
❖ **Advanced Interconnects**	- Flip-chip - Wire bonding - Ball Grid Array (BGA) - Quad Flat Package (QFP)	- Through-silicon vias (TSVs) - Hybrid bonding for high-density 2.5D/3D ICs - Micro-bump/pillar interconnects - Wafer-to-wafer bonding for heterogeneous integration	**Nilesh Badwe** (MsE, IIT K) **& Shiv Govind Singh** (EE, IIT H)

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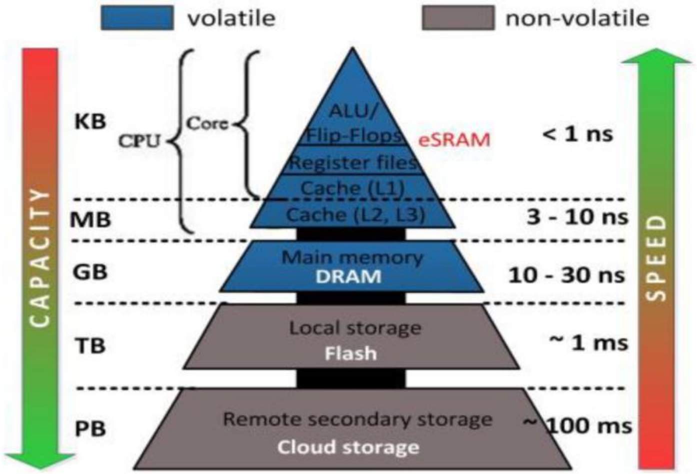
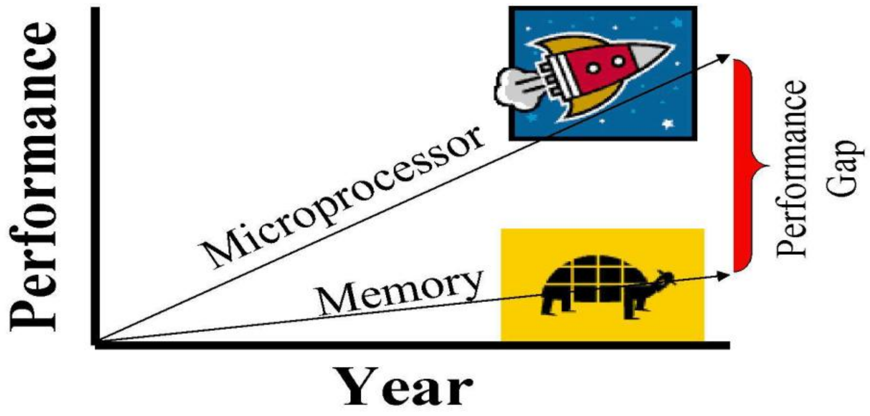
Devices Materials: Next-Gen Industry Needs and Technical Challenges

Today's concerns

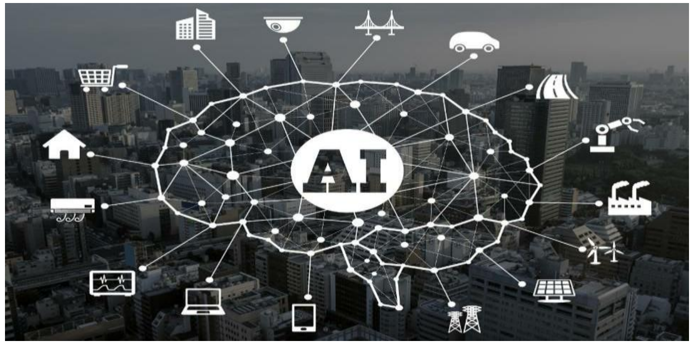




"Memory Wall" issue

?

Future Need



Need fast access of data

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The Era of Big Data — Major concerns

- **The ongoing shift from computation-centric to data-centric applications**: Growing numbers of cloud services and large data centers for platforms like Facebook, Google, Twitter, Instagram. . . demand prompt access to any data at any time

- **Reducing energy consumption:** About 50% of the electrical energy consumption of data centers is used for cooling. Moreover, 5–7% of global electrical energy is consumed by computing devices

- **Closing the memory gap:** Large amounts of data have to be kept at immediate access. The access time difference between long-term mass storage and RAM becomes more and more crucial

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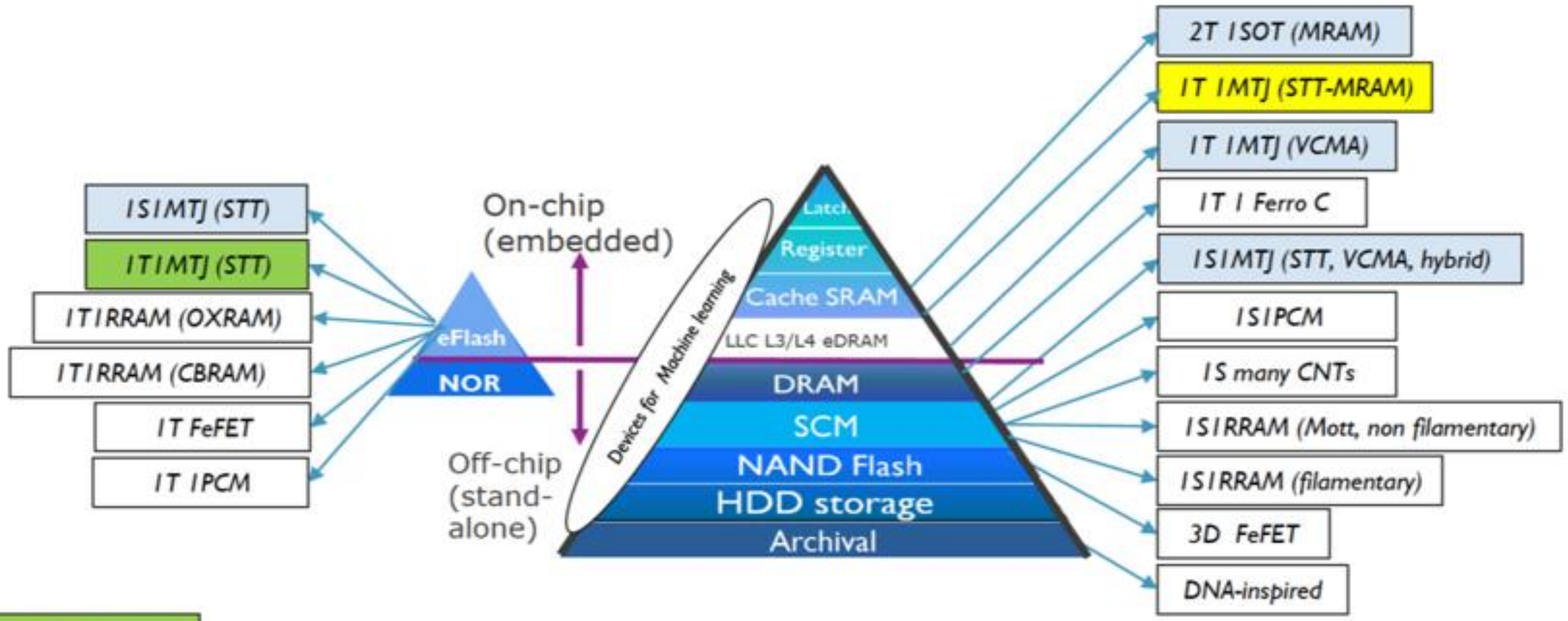
Emerging memory technology by potential application



🟩 Made it
🟨 Trying to make it
🟦 Research (or niche)

1S = 1 Selector
1T = 1 transistor
FeFET = Ferroelectric
STT = Spin transfer Torque
SOT = Spin orbit Torque
VCMA = Voltage Control Magnetic anisotropy

imec imw 2020

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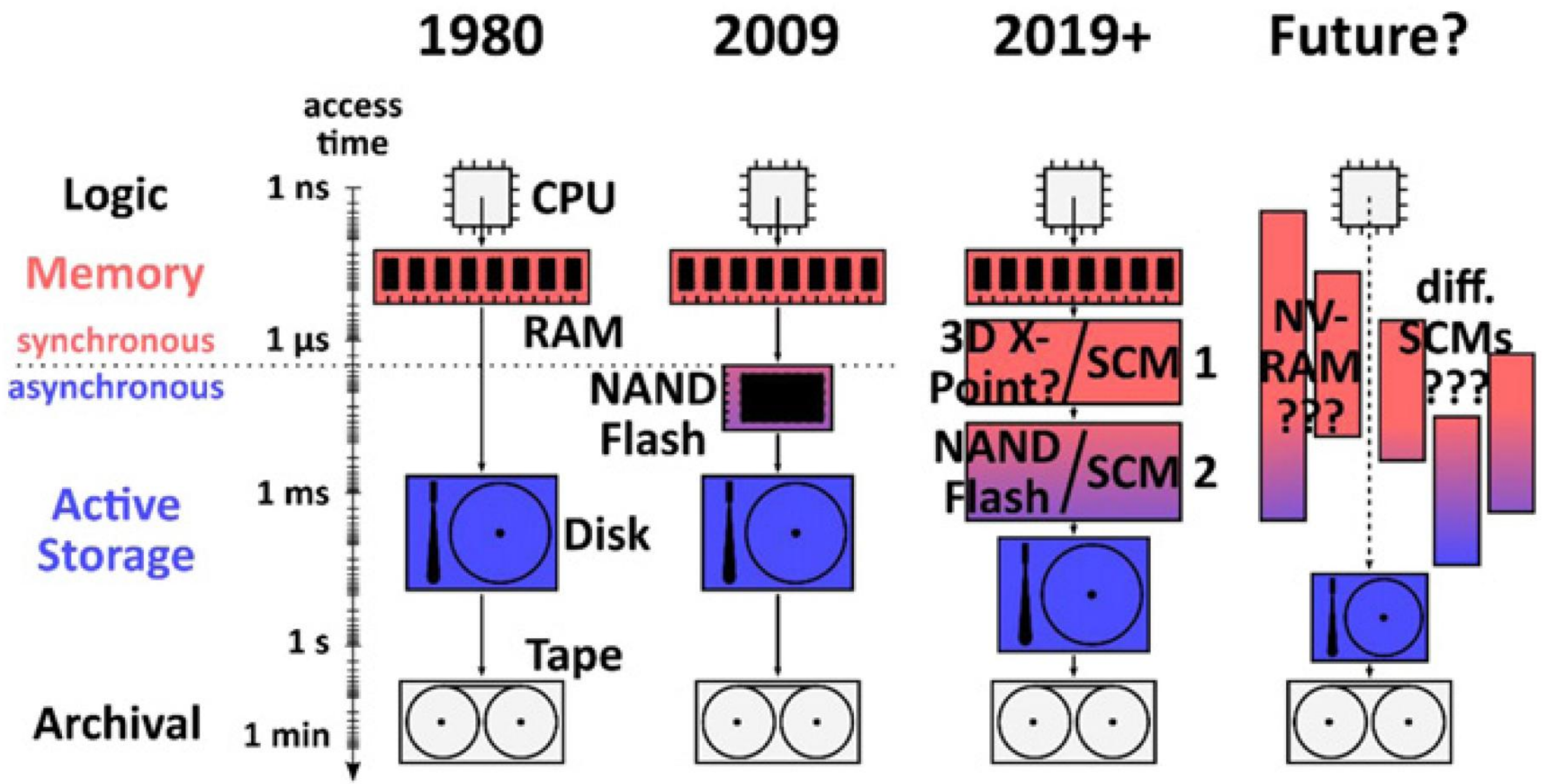
Market trends and drivers



Reef: Rep. Prog. Phys. **83** (2020) 086501

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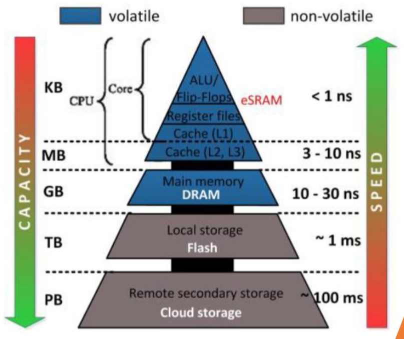
Devices Materials (Beyond-CMOS): Research Vision

Proposed Approach

Current Approach



Classical

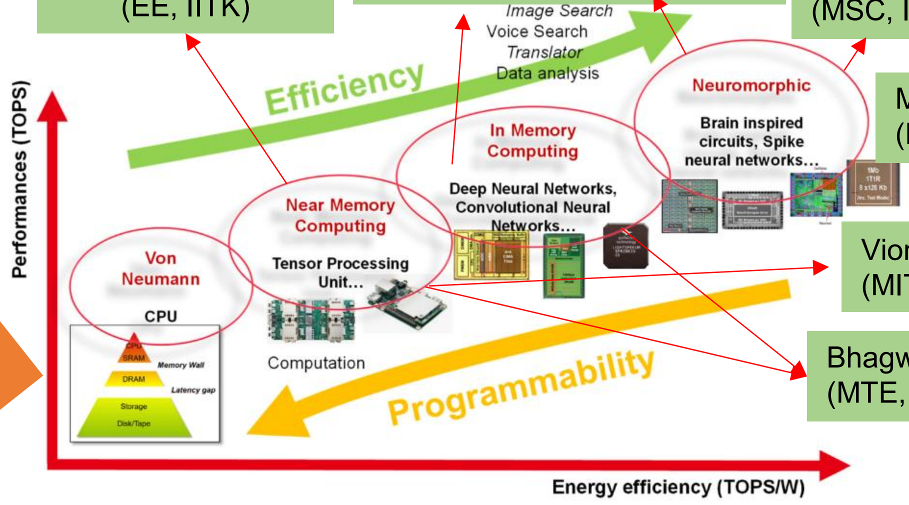
Quantum

Emerging Memory and Computing Platform

Shubham Sahay
(EE, IITK)

Debanjan Bhowmik (EE, IITB)

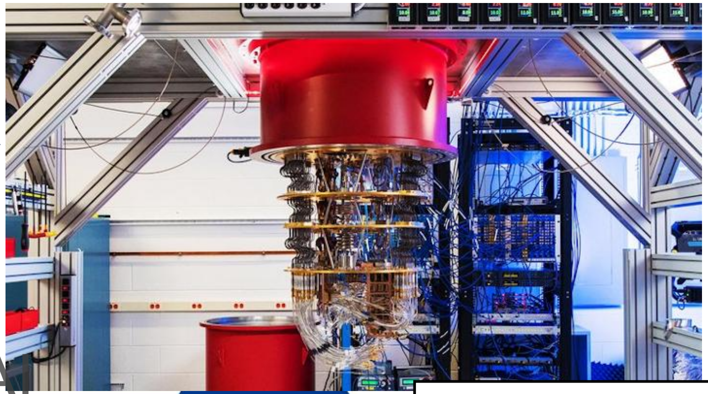
Ayan R. Chaudhuri
(MSC, IIT Kgp)



Murali K P
(NIT Calicut)

Viond Joshi
(MIT, Manipal)

Bhagwati Prasad
(MTE, IISc)



Google's new TensorFlow Quantum tool lets developers build quantum AI models

Quantum Materials

Bhagwati Prasad
(MTE, IISc)

Pranab Muduli
(MTE, IISc)

C. Murapaka
(MSME, IIT Kgp)

Devices Materials for Cryogenic Computing Platform

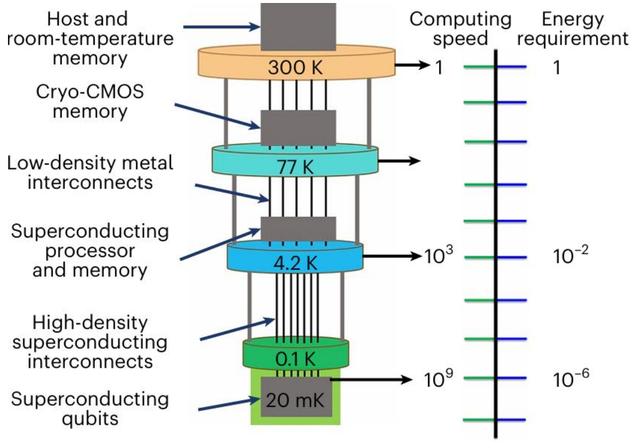
Pranab
Muduli
Phy, IITD

Bhagwati
Prasad
(MTE, IISc)

Abhisek
Dixit
(EE, IITD)

Debanjan
Bhowmik
EE, IITB

Classical-Quantum Interface



Nature Electronics, 6 (2023)

Packaging Materials Solution for Quantum Platform

Praveen Kumar
(MTE, IISc)

Praveen Ramamurthy
(MTE, IISc)

Madhusudan Singh
(EEE, IIT Delhi)

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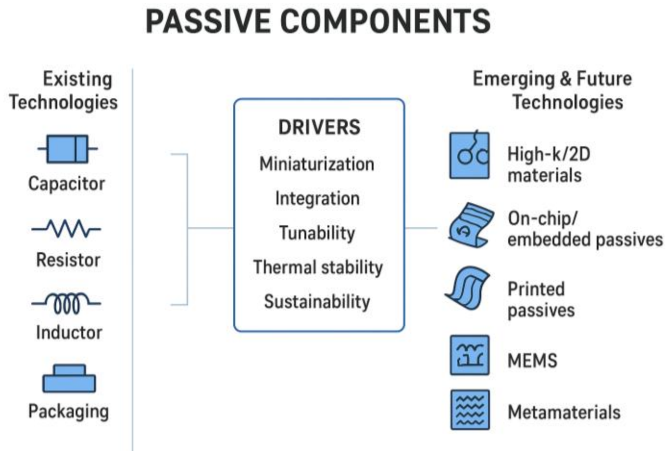
Passive Components — Existing vs Proposed Emerging: Materials Technologies

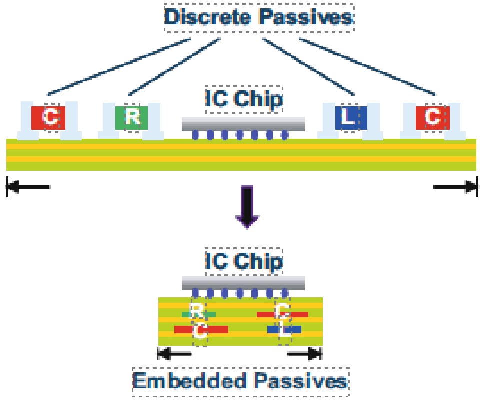


PASSIVE COMPONENTS

Existing Technologies
- Capacitor
- Resistor
- Inductor
- Packaging

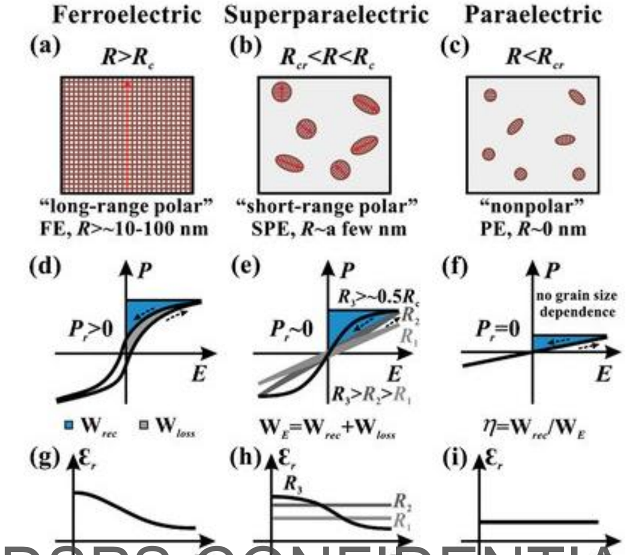
DRIVERS
- Miniaturization
- Integration
- Tunability
- Thermal stability
- Sustainability

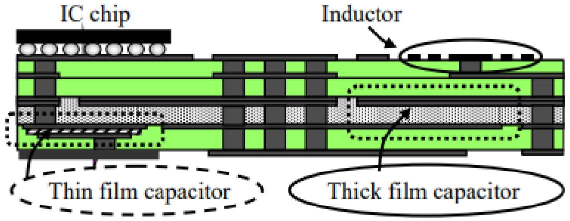
Emerging & Future Technologies
- High-k/2D materials
- On-chip/ embedded passives
- Printed passives
- MEMS
- Metamaterials



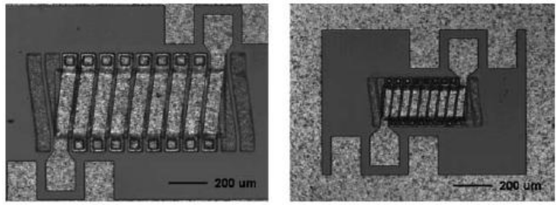
Trend

Materials for Capacitor – High Dk, Low Loss, Low TCC





Embedded Passives



Component	Traditional Materials/Performance	Latest Developments / Performance	Benefits of Latest Developments
Resistors	Carbon/metal film, tolerance ~1-5%, power ratings few watts	Graphene, carbon nanotube resistors with higher precision, enhanced thermal management, smaller size	Higher precision, improved thermal stability, miniaturization
Capacitors	Ceramic MLCC, electrolytic capacitors, moderate ESR	Nanostructured dielectrics, conductive polymer capacitors, lower ESR, higher capacitance density	Increased energy density, better voltage tolerance, low ESR
Inductors	Ferrite cores, lower efficiency at high frequency	Nano-material based inductors, advanced magnetic cores for high frequency, low loss	Better high-frequency performance, smaller footprints

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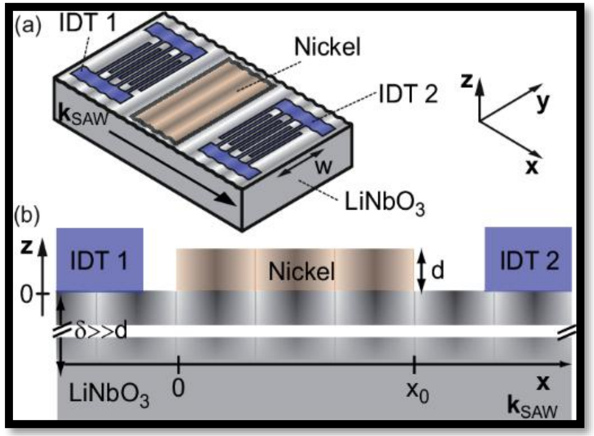
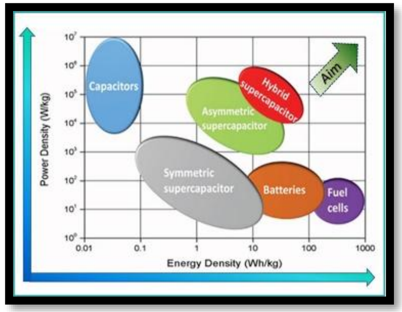
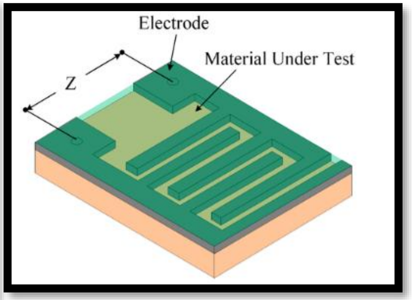
Passives on Chip

AI and IOT Materials and Devices: Sensors, Filters, Resonators, Oscillators, Capacitors, Power and Computing Devices

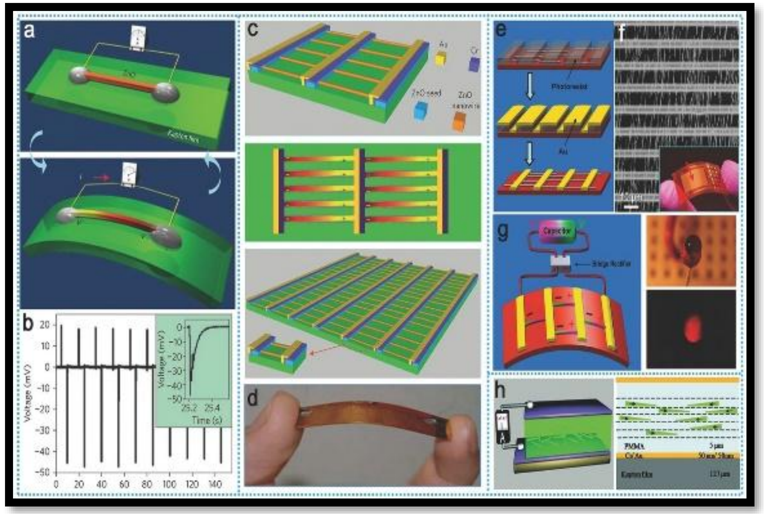


ADFMR Magnetic sensor



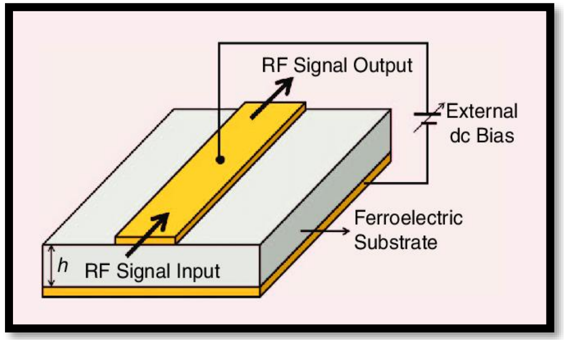


Ceramic Supercapacitors



Piezoelectric sensors

Phase shifter and MW filter



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Multidisciplinary India-wide Faculty Team with Expertise in Strategic Areas

Core Faculty Team


Bhagwati Prasad (MTE, IISc)
Device Materials


Murali K P (ME, NIT Calicut) – Co-Lead
Dielectric and Magneto-dielectric


Deepak Arora
(CE, IIT J)
Polymer dielectrics, ‘Electronic Packaging


Ayan R. Chaudhuri
(MSC, IIT Kgp)
Functional Oxide Materials


Madhusudan Singh
(EEE, IIT Delhi)
Printed and solution-processed low-cost material synthesis


Praveen Kumar
(MTE, IISc) – Co-lead
Electromigration, Packaging Materials,


Praveen Ramamurthy
(MTE, IISc)
Organic Materials


Chandrasekhar Murapaka
(MSME, IIT Kgp)
Magnetic Materials


Suryasarathi Bose
(MTE, IISc)
Polymer and EMI shielding materials

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Cross-ICC Faculty with relevant expertise


Ankush Bag
(EE, IIT G)
GaN power devices


Anandaroop Bhattacharya
(ME, IIT Kgp)
Thermal management


Pradeep Dixit
(ME, IIT B)
Substrates



Nilesh Badwe & Shiv Govind Singh
(MsE, IIT K) & (EE, IIT H)
Interconnects, die-attach



Parlapalli V Satyam & Akshay K
(EE, IIT Bhub.)
SiC power devices


Shiladri Chakraborty
(EE, IIT B) - Lead
Power electronics, SiC pkgng.


Naresh Emani
(EE, IIT H)
Optoelectronic drive


Abhisek Dixit
(EE, IITD)
CMOS Devices

Global Academic Collaborators

Prof. Raj Pulugurtha
(Florida International University)
Expertise: Packaging Materials

Research Expertise: Electronic and Bioelectronic Packaging, Flex and 3D packaging with Heterogeneous System Integration for Emerging Biomedical, Communication and Computing systems, Wearable and Implantable Medical Devices, Advanced Passive Components, Vertical Power Delivery, 5G and 6G Systems Packaging, Antenna Sensor Integration, Power and Data Telemetry, Hermetic Packaging, Interconnects and Connectors

Prof. R Ramesh
(Rice University)
Expertise: Beyond CMOS Memory Materials

Research Expertise: Atomic-scale synthesis of complex oxide heterostructures, 2D materials, spin-charge coupling, Ferroelectrics and Spintronics, electron microscopy, piezoforce microscopy, NV magnetometry, materials processing for devices, energy efficient electronics

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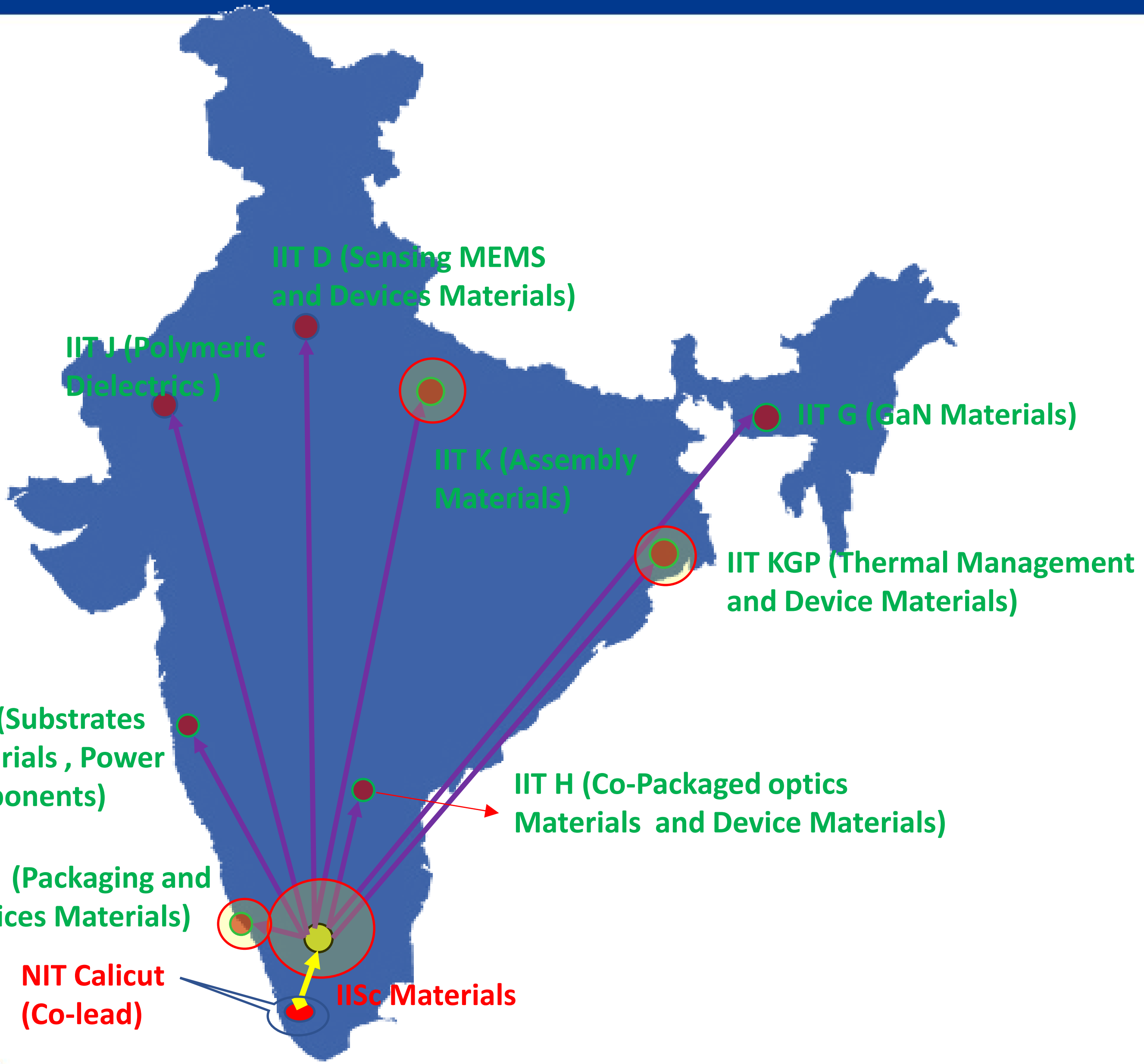
Materials: Primary & Satellite Centers

ICC: HUB & SPOKE MODEL



IIT D (Sensing MEMS and Devices Materials)

IIT J (Polymeric Dielectrics)

IIT K (Assembly Materials)

IIT G (GaN Materials)

IIT KGP (Thermal Management and Device Materials)

IIT B (Substrates Materials , Power components)

IIT H (Co-Packaged optics Materials and Device Materials)

MIT (Packaging and Devices Materials)

NIT Calicut (Co-lead)

IISc Materials

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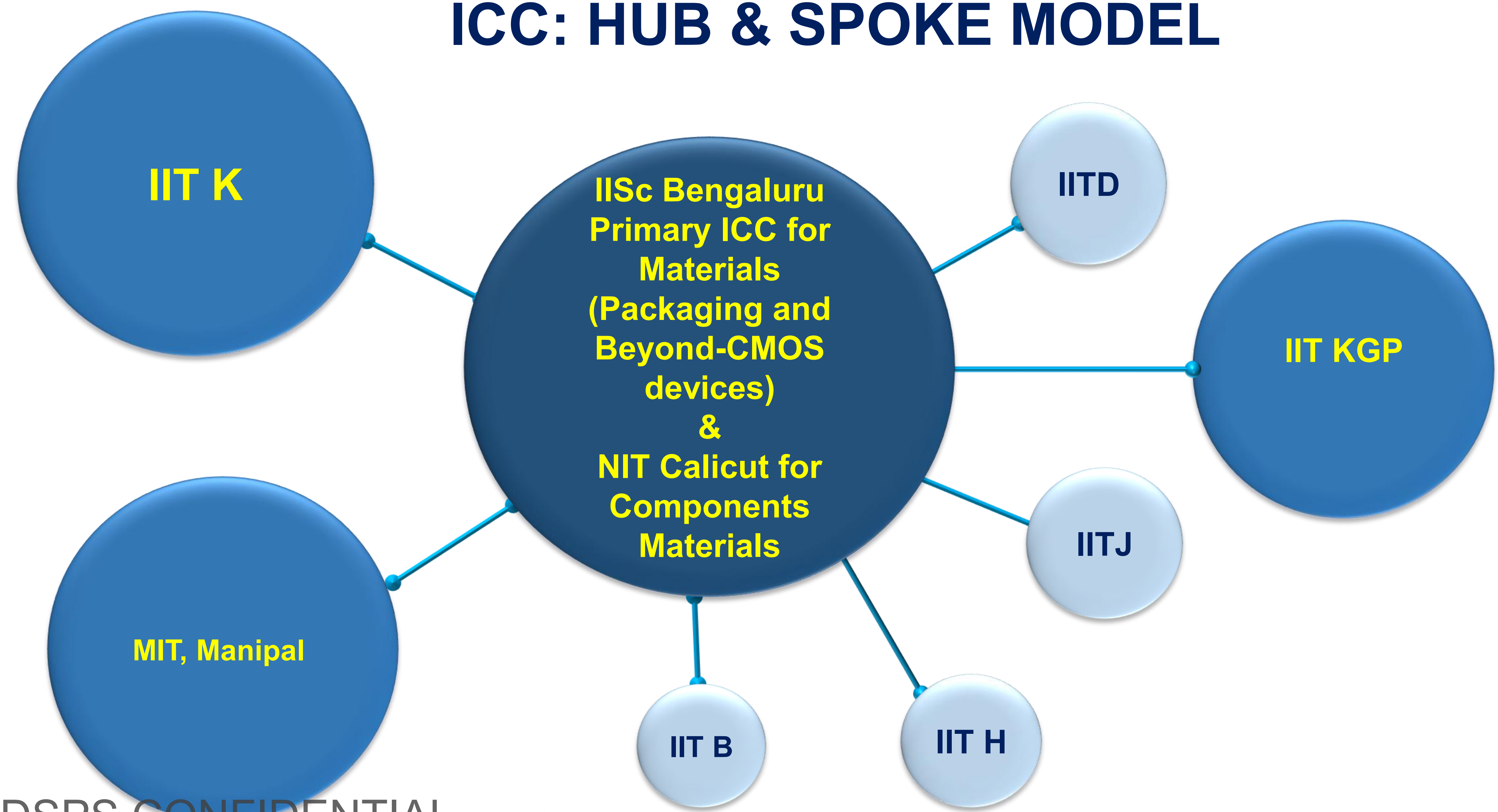
ICC: HUB & SPOKE MODEL



IISc Bengaluru
Primary ICC for
Materials
(Packaging and
Beyond-CMOS
devices)
&
NIT Calicut for
Components
Materials

IIT K

IITD

IIT KGP

IITJ

IIT H

IIT B

MIT, Manipal

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Global Industry Partners

Currrently interested industry partners

- Infineon
- MacDermid Alpha
- Corning
- AMD
- Tata Electronics
- TI
- Indium
- Lam Research
- Applied Materials
- Delta Electronics

Potential future industry partners

- Micron
- Western Digital
- Intel
- Honeywell
- IBM
- ST Micro
- Vedanta
- SiC Power
- Henkel
- Semikron
- Vishay
- Fuji
- Mitsubishi Electric
- Toshiba
- NXP Semi
- Micro Semi
- Rogers
- Kyocera
- TDK
- Danfoss
- Dupont
- Heraeus Electronics
- Bosch
- Denka
- Semicosil

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Education Programs: Materials (Packaging and Beyond CMOS devices)

On-going and proposed courses

1. Materials: Synthesis and Characterization
2. Packaging materials
3. Device Fabrication and Characterization
4. Memory materials and devices
5. Magnetic memory devices
6. Memory-logic 3D IC
7. Neuromorphic Computing, Edge Artificial Intelligence, Nanomagnetism and spintronics
8. Logic-Memory for In-Memory-computing
9. Bioinformatics and DNA-based storage technology
10. Memory technology and Neuromorphic computing –system level (Lectures are available in Youtube)
11. Advance channel engineering and system architecture
12. Emerging memory technology
13. Novel data storage technology
14. AI/ML for memory technology
15. Packaging and Integration –Industry expert Material

Education Programs

1. Offering summer school/ winter school/ workshop etc.
2. Individual courses for B. Tech. and M. Tech.
3. Online diploma program
4. Short courses on individual topics
5. Hand-on training programs
6. Dedicated certificate courses for industry professionals
7. Online certificate courses: Academia and Industry
8. Exchange programs: both intra India and international that seed active collaborations in these fields, and develop skills to researchers.
9. Online M.Tech. degree program (Semiconductor packaging and device materials)

Expected Workforce Development

Year	5 Years	10 Years
PDPs*	400	800
B Techs	350	700
M Techs	150	300
PhDs	50	100
Total	1000	2000

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Materials Development Process Flow

Materials growth

- Infrastructure development
- Spin coater
- Sputtering cluster tool
- Electrodeposition
- Atomic Layer Deposition
- Chemical Vapour Deposition
- Fume hoods

Materials Characterizations

- AFM/PFM/MFM
- Ferroelectric testers
- Raman Spectroscopy
- PPMS
- XPS
- X-Ray Diffractometer
- VNA with accessories
- Chalk Tester
- Impedance analyzer

Creation of test structures

- Basic Photolithography
- Ion Beam Milling
- RTA
- Evaporator
- Focused Ion Beam
- Wet bench
- Laser beam

Testing and Integration

- Wafer bonder
- Probe Stations with basic electronics
- Parameter Analyzer
- Optical Microscope

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Budget Overview

Category	Year 1	Year 2	Year 3	Year 4	Year 5	Total
1. **Infrastructure Facility – Hub** (including annual maintenance)	60 + 2Cr	15 + 2 Cr	10 + 2 Cr	2 Cr	2 Cr	95 Cr
2. **Research Projects Cost** (15 Projects @20 lakhs/annual)	3 Cr	3 Cr	3 Cr	3 Cr	3 Cr	15 Cr
3. **Global Collaborators** (x2)	2 Cr	2 Cr	2 Cr	2 Cr	2 Cr	10 Cr
4. **Students** (15 Ph.D. + 15 M.Tech. + 15 B.Tech.)	1 Cr	1 Cr	1 Cr	1 Cr	1 Cr	5 Cr
5. **Education & Workforce** Technology workforce Manufacturing workforce	 50 lakhs 50 lakhs	 50 lakhs 50 lakhs	 50 lakhs 50 lakhs	 50 lakhs 50 lakhs	 50 lakhs 50 lakhs	5 Cr
6. **Manpower**						5 Cr
Full-Time Research Faculty (x2)	50 lakhs	50 lakhs	50 lakhs	50 lakhs	50 lakhs	
Company Engineers on Campus	-	-	-	-	-	
Manager of Operations (x1)	25 lakhs	25 lakhs	25 lakhs	25 lakhs	25 lakhs	
Central Secretary (x1)	12 lakhs	12 lakhs	12 lakhs	12 lakhs	12 lakhs	
Manager of Finance (x1)	13 lakhs	13 lakhs	13 lakhs	13 lakhs	13 lakhs	
7. **Travel** (travel to industry partners, travel to international conf.)	50 lakhs	50 lakhs	50 lakhs	75 lakhs	75 lakhs	3 Cr
8. **Infra for satellite centers (IIT KGP, IIT K, MIT (Manipal))**	15 Cr	5 Cr	5 Cr	-	-	25 Cr

Total ≈163 Cr

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List of R&D projects

No.	Project title	Lead PI
1.	Materials for Tunable Shock Absorption in Next Generation Microelectronic Packages	Prof. Praveen Kumar (IISc); Email: praveenk@iisc.ac.in
2.	Development of 2D Materials-based Thermal Interface Materials for Enhanced Cooling	Prof. Pradeep Dixit (IIT B); Email: pradeep.dixit@iitb.ac.in
3.	Advanced Functional Materials for AI, IoT and Sensing Applications	Prof. Bhagwati Prasad (IISc); Email: bpjoshi@iisc.ac.in
4.	Systematic study of temperature-dependent properties of Sn-Bi-based low-temperature solder alloys with various alloying elements	Prof. Nilesh Badwe (IITK); Email: nbadwe@iitk.ac.in
5.	Harnessing Ferroelectric HfZrO2 for Advanced Non-Volatile Memory in AI Applications	Prof. Bhagwati Prasad (IISc); Email: bpjoshi@iisc.ac.in
6.	Beyond Moore: Materials Development for Compute-In-Memory (CIM) Devices	Prof. Ayan R. Chaudhuri (IIT Kgp); ayan@matsc.iitkgp.ac.in
7.	Biodegradable EMI Shielding Materials to mitigate E-waste	Prof. Suryasarathi Bose (IISc); Email: sbose@iisc.ac.in
8.	Polymeric Dielectrics for Build-Up Layers Enabling 1 µm Fine Line Space in HDI Substrates for Large Area Processing	Prof. Deepak Arora (IIT J); Email: deepakarora@iitj.ac.in
9.	Lead-free solder and interconnect materials with low sintering temperatures	Prof. M Singh, (IIT D); Email: msingh@ee.iitd.ac.in
10.	Ultra low permeable encapsulant for Packaging	Prof. P C Ramamurthy (IISc); Email: praveen@iisc.ac.in
11.	Energy-efficient non-volatile memory (NVM) technology using topological insulators	Prof. C Murapaka(IIT H); Email:mchandrasekhar@msme.iith.ac.in
12.	Bio-degradable RFID Tags	Prof. Subho Dasgupta (IISc); Email: dasgupta@iisc.ac.in
13.	Next Generation Non-Volatile In-Memory Computation	Prof. V K Joshi (MIT, Manipal); Email: vinodkumar.joshi@manipal.edu
14.	Thermal Aware Material Selection and Design-modeling of Advanced IC Packages to Improve Electronics Reliability	Prof. Ribu Mathew (MIT, Manipal); Email: ribu.mathew@manipal.edu
15.	Disposable Energy Sources for Self-powered Wearable Devices	Prof. Amit K. Goyal, MIT, Manipal; Email:ribu.mathew@manipal.edu
16.	Design, fabrication and characterization of power inductors on glass substrate packages with high inductance densities and quality factor employing ferromagnetic materials	Prof. Vasu Pulijala (VNIT Nagpur); Email: p.vasu@ece.vnit.ac.in

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List of R&D projects

No.	Project title	Lead PI
17.	Design, fabricate, characterize and demonstrate high-performance 5G-to-6G/Sub-THz antenna arrays in ultrathin (200 microns) form-factors with MTM super structure.	Dr laitkumar (ECED, NITC), lalit@nitc.ac.in
18	Design, fabrication and characterization of high frequency power inductors using magnetic vortex materials	Dr Ashiq Muhammed (EED, NITC) ashiqmuhammed@nitc.ac.in
19.	Design, fabrication and characterization of super paraelectric (SPE) state thin films on glass substrate with high capacitance densities and quality factor employing MIM geometries and tunable hybrid compounds.	Dr Vinod E Madhavan (DMSE, NITC), vinodem@nitc.ac.in
20	Development of EMI shielding in Mixed signal packages - Both for Internal component-component & External package-package isolation	Dr Murali K P (MED, NITC), komurali@nitc.ac.in

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Technology workforce education programs

Milestones	Year 1	Year 2	Year 3	Year 4	Year 5
Submit Proposal	🟩				
Identify industry partners	🟩				
Set up industry consortium	🟩	🟩			
Set up infrastructure		🟩	🟩		
Develop Research Programs		🟩	🟩	🟩	🟩
Develop Educational Programs		🟩	🟩	🟩	🟩
Demonstrate Technologies			🟩	🟩	🟩
Integrate Technologies into Industry Prototype 1			🟩	🟩	🟩
Integrate Technologies into Industry Prototype 2				🟩	🟩
Integrate Technologies into Industry Prototype 3					🟩

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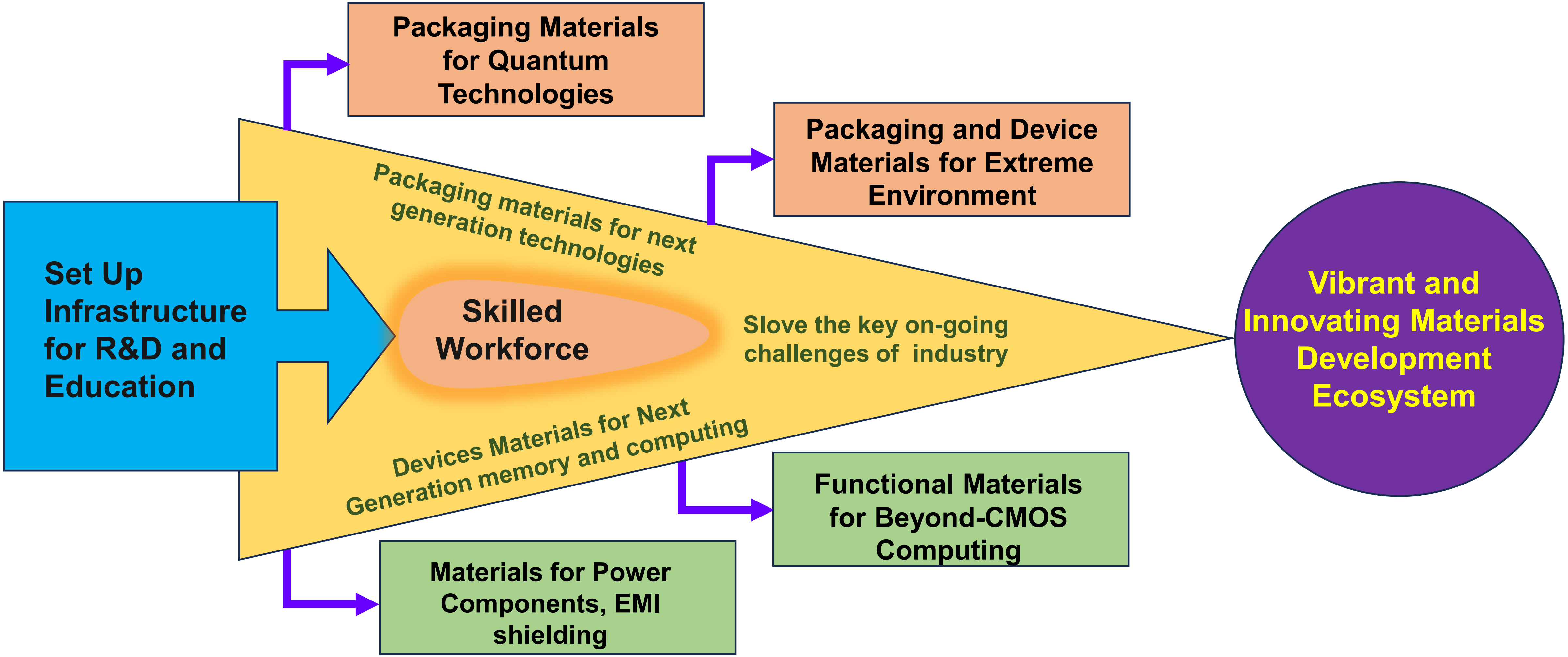
Summary: Sustainable Ecosystem for Materials ICC



Set Up Infrastructure for R&D and Education

Skilled Workforce

Packaging materials for next generation technologies

Slove the key on-going challenges of industry

Devices Materials for Next Generation memory and computing

Packaging Materials for Quantum Technologies

Packaging and Device Materials for Extreme Environment

Functional Materials for Beyond-CMOS Computing

Materials for Power Components, EMI shielding

Vibrant and Innovating Materials Development Ecosystem

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Description of proposed R&D projects (Materials)

Project 1: Materials for Tunable Shock Absorption in Next Generation Microelectronic Packages

PI: Praveen Kumar, Suryasarathi Bose and Abha Misra (IISc Bengaluru)

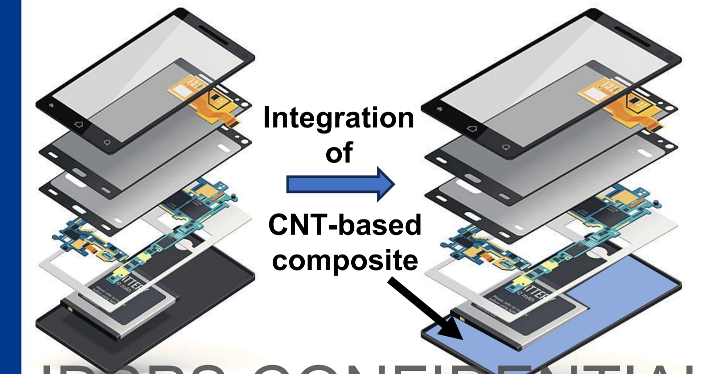
Objective: Develop CNT-based composite materials with tunable shock absorption capacity for protecting high-density packages at wide range of temperatures and strain rates

Proposed vs. Prior Art

	Current state	Proposed
Shock absorption	External cover	Integral part, small form factor
Multi-functionality	Multiple materials for EMI, TIM and shock absorption	Single composite material
Temperature sensitivity	Temperature dependent	CNT properties don't depend on temperature over wide range of temperatures

Approach

1. Integration of nominally vertically-aligned CNT foam and sensitive components of a package
2. Partial impregnation of CNT foam with EMI-grade, TIM-grade polymeric materials
3. Integration of an intelligent electric circuit (existing battery derived power) to get activated upon sensing a free fall or an impact
4. Validation using a densely packed mobile devices over a wide range of temperature


Integration of
CNT-based composite

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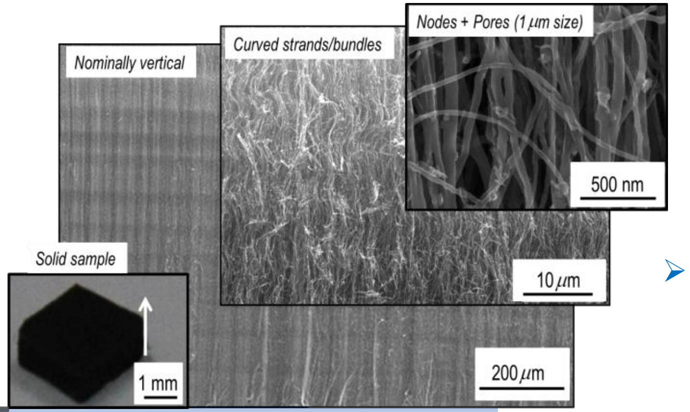
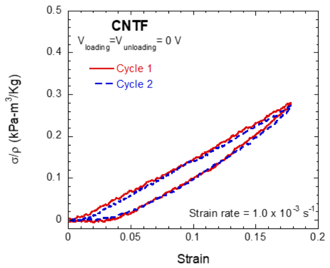
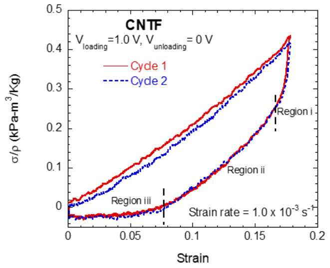
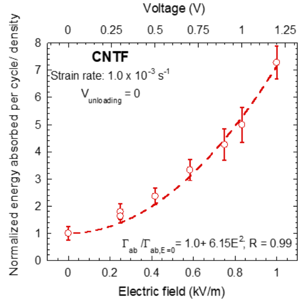








- ➢ CNT foam has hierarchal length scales → Scope of forming composites with multiple classes of materials
- ➢ Almost an order of magnitude increase in energy absorption with 1 V applied over 1 mm thick CNT foam

Outcome and Impact

- ➢ Robust performance under impact conditions, without needing any additional power sources and hardware
- ➢ Minimization of components in a material for multi-functionality, resulting in further reduction in form factor

Project 2: Development of 2D Materials-based Thermal Interface Materials (TIM) for Enhanced Cooling

PI: Pradeep Dixit (IIT Bombay)

Objective: Develop a Carbon-based materials (Graphene/CNT/MoS_2) based Thermal Interface Materials (TIM) to achieve a 10x higher heat dissipation in high-density electronic packaging applications.

Outcome and Impact:

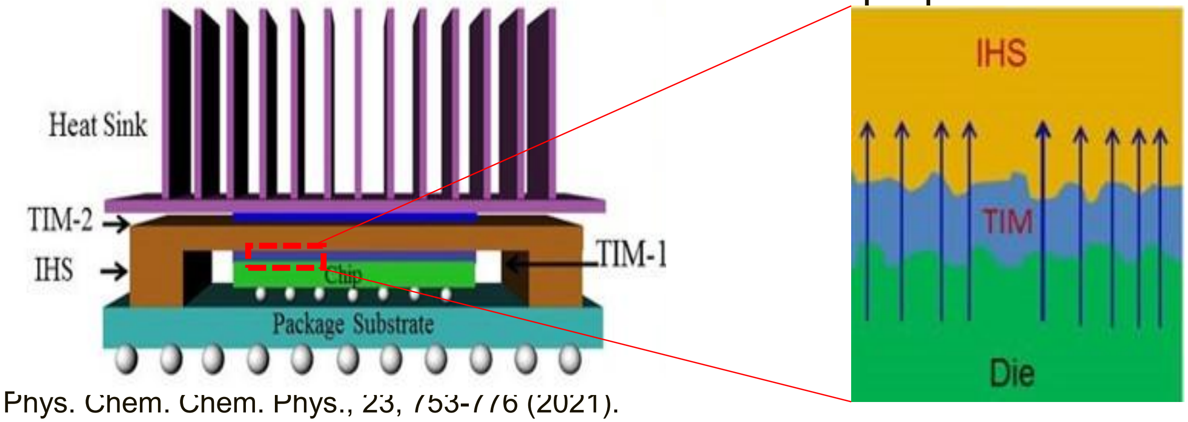
- Demonstration of advanced Carbon-materials /MoS_2 based thermal interface material (TIM)
- Design, synthesis, and characterization methodology
- Significant reduction in thermal resistance

Approach:

- Growing vertically oriented array of metallic CNTs
- Transferring the CNTs array and mixing with epoxy polymer
- Fabrication of a daisy-chain-like test structures for measurement of adhesion and thermal properties.

Proposed vs. Prior Art

	Current state	Proposed
TIM	Ceramic Particles in Epoxy	Graphene/ Vertical-aligned CNTs/ MoS2 in epoxy
Effective in-plane thermal conductivity	1.5-10 W/m-K	20 W/m-K



1. Zhang et al, "Recent progress in the development of thermal interface materials: a review", Phys. Chem. Chem. Phys., 23, 753-776 (2021).
2. Ma et al, "Strategies for enhancing thermal conductivity of polymer-based thermal interface materials: a review", J. Mat. Sci., 56, pp. 1064 (2021)
3. Lv et al, "A mini review: application of graphene paper in thermal interface materials", New Carbon Mat., 36, pp. 930 (2021)

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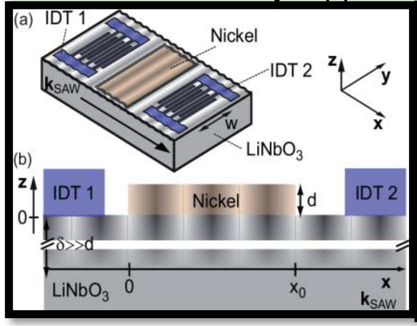
Proposal 3: Advanced Functional Materials for AI, IoT and Sensing Applications

PI: Bhagwati Prasad (IISc Bengaluru)

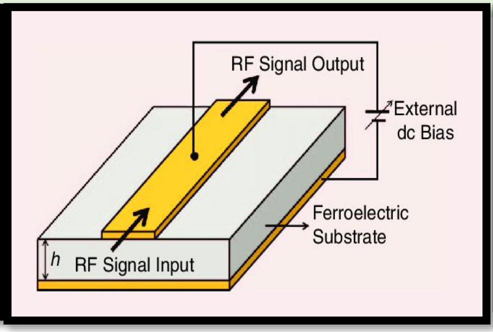
Co-PI: Chandrasekhar Murapaka (IITH) & Praveen Ramamurthy (IISc Bengaluru)

Objective:

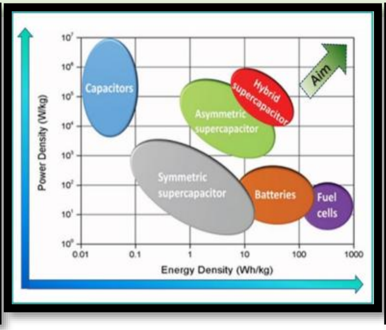
- Development of magnetic sensor that can detect pico (pT) to femto Tesla (fT) range of magnetic field.
- Development of novel piezoelectric materials for bio-medical and energy harvesting applications.
- Development of ferroelectric material (e.G. HfO_2,AlSnN etc.) Based phase shifters and tunable microwave filters (300 Mhz ~ 300Ghz) for communication and satellite applications.
- Ceramic (such as $bifeo_3$,and $HfZrO_2$ etc.) Based high-energy-density supercapacitor for power electronics and military applications.



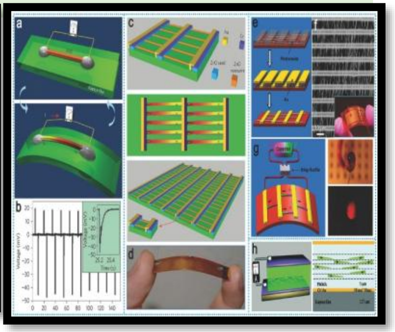
ADFMR Magnetic sensor



Phase shifter and MW filter



Ceramic Supercapacitors



Piezoelectric sensors

Approach

- Material Synthesis and Characterization: Develop new composite materials and analyze their structures and properties using techniques like X-ray diffraction and scanning electron microscopy to ensure optimal performance.
- Device Fabrication and Integration: Utilize advanced fabrication techniques such as lithography and thin-film deposition to construct sensor devices and components from synthesized materials.
- Performance Testing and Optimization: Test device performance extensively and use results to refine materials and structures, enhancing functionality like tunability and power density.
- Cost Analysis and Scalability Assessment: Conduct thorough cost analysis and scalability tests to ensure the economic viability and industrial applicability of the production processes.

Outcome and Impact:

- **Cost-Effective, High-Performance Materials**: Lower-cost, efficient sensors and capacitors for AI, IoT, and sensing applications, making these technologies more accessible and driving broader adoption in various industries.
- **Enhanced Tunability and Power Density**: Improved energy storage and efficiency in electronic devices, leading to advancements in sustainable energy solutions and portable systems.

Technology	Current state	Proposed
Magnetic sensors	Costly (~$10K /unit) 1fT at cryogenic condition only.	Cheapest (~$1-$10) 10^{-12} to 10^{-15} tesla at RT
Piezoelectric sensors	Cheap (~$10-$100 /unit) Power density ~30 Wcm^{-2}	Cheapest (~$1-$10 /unit) Power density ~490 Wcm^{-2}
Ferroelectric capacitors for MW filters	~48% tunable	Up to 90% tunability
High energy density Ceramic based supercapacitors	Power density ~kW/kg	Power density ~MW/kg

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References:

- C. Dong et al., "Thin Film Magnetoelectric Sensors Toward Biomagnetism: Materials, Devices, and Applications," *Advanced Electronic Materials*, 2200013 (2022).
- B. Prasad et al., "Ultralow Voltage Manipulation of Ferromagnetism," *Advanced Materials*, 32, 2001943, (2020)

Project 4: Systematic study of temperature-dependent properties of Sn-Bi-based low-temperature solder alloys with various alloying elements

Nilesh Badwe (IITK), Pradipta Ghosh (IITGN), Shiv Govind Singh (IITH)

Objective

To create a knowledge base of the impact of different alloying elements and their concentrations on the physical and mechanical properties of SnBi based low temperature solders (LTS) over a temperature range relevant to electronics

Approach

- **Synthesis** of the Sn-Bi-based LTS Solder doped with Ag, Cu, Sb, In, Co, and Ni with concentrations 0-1 wt.% respectively
- **Microstructural Characterization:** IMC thickness/composition on CuOSP and ENIG substrate coupon pre and post ageing
- **Physical properties:** Resistivity, Temperature coefficient of resistance, Melting and solidification behaviour
- **Thermomechanical Properties:** Tensile testing and low cycle fatigue testing at (-40°C, -20°C, 0°C, 25°C, 85°C, 100°C)

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Proposed vs Prior Art

Parameters	Composition	Current state of Art	Proposed
Temperature-dependent tensile properties	Eutectic Sn-58Bi	Limited	Yes
	Other alloying elements	No	Yes
Temperature-dependent fatigue performance	Eutectic Sn-58Bi	No	Yes
	Other alloying elements	No	Yes
Temperature dependant resistivity	Eutectic Sn-58Bi	Limited	Yes
	Other alloying elements	No	Yes

Proposed Timeline

Activity and milestone	**Year 1**		**Year 2**		**Year 3**		**Year 4**	
	H 1	H 2	H 1	H 2	H 1	H 2	H 1	H 2
Test coupon design	🟩	🟩						
Alloy synthesis and melting/solidification assessment		🟩	🟩	🟩				
Temperature dependent resistivity measurement			🟩	🟩				
Shear fatigue study without current				🟩				
Effect of current density on shear fatigue life				🟩	🟩	🟩	🟩	
Model development							🟩	🟩
Data reporting		🟩		🟩		🟩		🟩

Kamaruzzaman, L.S. and Goh, Y., 2022. *Soldering & Surface Mount Technology*, *34*(5), pp.300-318.

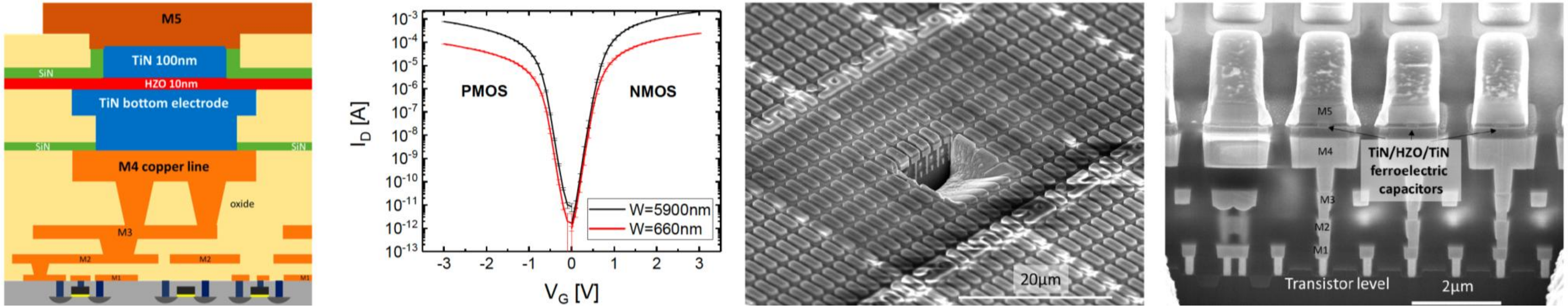
Mokhtari, O. and Nishikawa, H., 2016. *Materials Science and Engineering: A*, *651*, pp.831-839.

Project 5: Harnessing Ferroelectric $HfZrO_2$ for Advanced Non-Volatile Memory in AI Applications

PI: Bhagwati Prasad (IISc Bengaluru); Co-PIs: Ayan Roy Chaudhuri (IIT Kharagpur), Arabinda Haldar (IITH)

Objective: Develop and optimize the ferroelectric properties of Hf0.5Zr0.5O2 materials to create scalable, efficient, and durable non-volatile memory devices that enhance the performance and capabilities of AI technologies.

1T-1C integration of HZO capacitors down to 300nm diameter in the BEOL of 130nm CMOS node



Parameter	Current State of the Art	Proposed Advancements
Ferroelectric Material	Limited options with scalable issues, mainly based on perovskite structures	Development and optimization of Hf0.5Zr0.5O2 with superior scalability and stability
Endurance (Switching Cycles)	Typically up to 10^10 cycles	Increase endurance to ≥10^15 cycles, ensuring long-term reliability
Switching Speed	Around 100 ns	Improve to ≤10 ns
Energy Efficiency	High energy consumption per switching cycle (write ~ pJ/bit)	Drastically reduce energy consumption (~ aJ/bit)
Operating Voltage	Typically around 3V	Reduce to ≤1V to minimize power consumption and improve device safety
Material Homogeneity	Variability in material properties across batches	Ensure high levels of material homogeneity to guarantee consistent device performance

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Approach

- ☐ **Material Synthesis**: Develop $Hf_{0.5}Zr_{0.5}O_2$ with advanced deposition techniques, exploring doping to enhance properties.
- ☐ **Device Fabrication and integration**: Integrate material into memory architectures for improved efficiency.
- ☐ **Performance Testing**: Assess endurance and optimize electrical properties.
- ☐ **Scalability Analysis**: Evaluate production scalability and conduct cost assessments.

References:

- T. Francois et al., "Demonstration of BEOL-compatible ferroelectric Hf0.5Zr0.5O2 scaled FeRAM co-integrated with 130nm CMOS for embedded NVM applications," *IEDM*, 2019.
- B. Prasad et al., "Large tunnel electroresistance with ultrathin Hf0.5Zr0.5O2 ferroelectric tunnel barriers," *Advanced Electronic Materials*,. 7, 2001074, 2021.
- Z. Zhang et al., "Phase transformation driven by oxygen vacancy redistribution as the mechanism of ferroelectric Hf0.5Zr0.5O2 fatigue," *Advanced Electronic Materials*, 2300877, 2024.
- B. Prasad et al. "Ferroelectric field effect transistors having enhanced memory window and methods of making the same", US Patent 11,996,462, (May 2024), Granted.

Project 11: Energy-efficient non-volatile memory (NVM) technology using topological insulators

PI: Chandrasekhar Murapaka (IITH)
Co-PIs: Arabinda Haldar (IITH) and Bhagwati Prasad (IISc)

Objective - (i) Develop magnetic heterostructure thin films to harness spin orbit torque (SOT) for MRAM; (ii) Demonstration of SOT-switching driven by emerging topological insulators

	Current state	Proposed
Voltage requirement in MRAM	~ 1.5 V	< 1 V
Endurance of MRAM	10^{15}	~ infinite
Writing speed of MRAM	10 ns	< 1 ns

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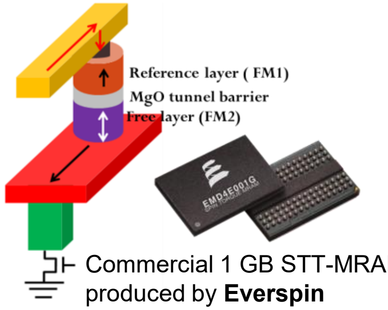
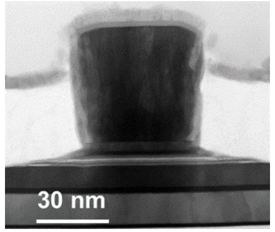
Approach

- Growth and optimization of materials with topological insulators (large spin orbit coupling) [Ref: Nature Comm. 12, 6251 (2021)]
- Demonstration of low power switching using SOTs with high spin Hall angle >>1 [Ref: Nature Materials 17, 808 (2018)]
- Demonstration of reading and writing of SOT memory in an MTJ pillar [Ref: IEEE VLSI Circuits 10.23919/VLSIC.2019.8778100]



Commercial 1 GB STT-MRAM produced by **Everspin**



Cross-section TEM image of MTJ stack (PRApplied 16, 024048 (2021))

Outcome and Impact

☐ Demonstration of SOT MRAM devices in cross-bar architecture with quasi-infinite endurance and ultra-high speed

☐ Replacement of SRAM and DRAM with spin based NVM

Project 13 : Next-Generation Non-Volatile In-Memory Computation

PI-Dr. Vinod Kumar Joshi, MAHE, Manipal

Objectives

1. Explore novel non-volatile MTJ device stacks and perform advanced micromagnetic simulations to **engineer parameters** that **enhance the efficiency of scalable memory cells**.
2. Develop a physics based compact model of the **optimized novel stack** using Verilog-A to accurately represent its electrical and magnetic behaviour.
3. Design and implement optimized **high-density in-memory arithmetic and logic circuits** to enhance performance for various applications (e.g., IoT, AI edge computing).

Entities	Prior Art	Proposed
Optimizing MTJ Stacks for Enhanced TMR and High PMA	CoFeB-MgO-CoFeB stacks with a 2.45 nm MgO layer show **limited PMA** ($\sim$1.3 mJ/m^2) **and Δ (40-50)** for high-density applications and exhibit asymmetric voltage bias dependence.	**LiF/MgO bilayer** tunneling barriers with LiF (0.15 nm) and MgO (2.3 nm) exhibit **high PMA** (2.8 mJ/m^2), leading to **Δ > 60** for data retention exceeding 10 years and **high TMR**, crucial for high-density applications (sub-10nm device).
Device Modelling	**Key Challenges:** Current MTJ models **lack the latest material and structure advancements** and struggle with scaling below 10 nm while maintaining reliability, TMR and thermal stability (Δ > 60).	Accurate device modeling parameters for high-density memory applications include the following ranges: 1. TMR: 100% to 300% 2. Speed: 1 to 10ns 3. Δ: 60-100 4. Retention: 10Y to > 20Y 5. Size: Below 10nm
In-memory Computing Circuits	Independent design, modelling and implementation.	Co-design enhances integration, optimizes performance, and improves parameter matching.

References:

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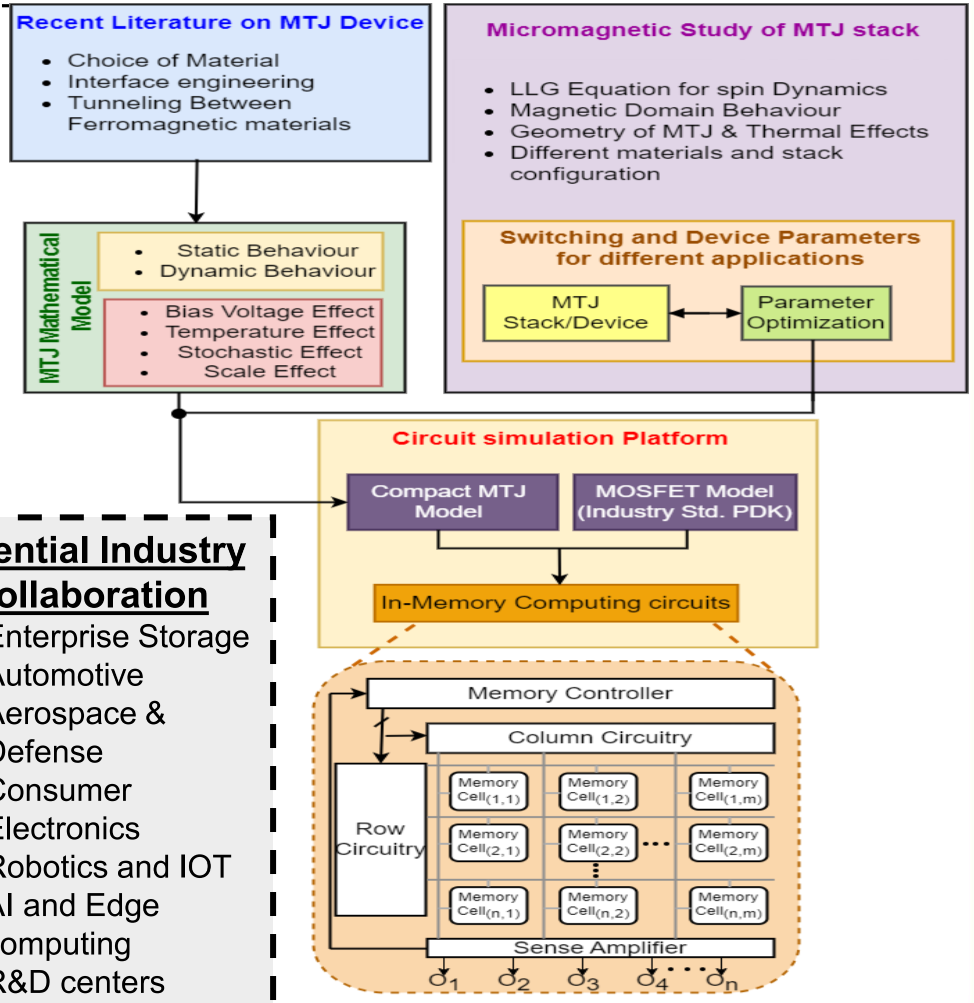
[1] https://www.snsinsider.com/reports/magneto-resistive-ram-mram-market-2315

[2] Nozaki, T., Nozaki, T., Yamamoto, T. et al. Enhancing the interfacial perpendicular magnetic anisotropy and tunnel magnetoresistance by inserting an ultrathin LiF layer at an Fe/MgO interface. NPG Asia Mater **14**, 5 (2022). https://doi.org/10.1038/s41427-021-00350-8

[3] Igarashi, J., Jinnai, B., Watanabe, K. et al. Single-nanometer CoFeB/MgO magnetic tunnel junctions with high-retention and high-speed capabilities. npj Spintronics **2**, 1 (2024). https://doi.org/10.1038/s44306-023-00003-2

APPROACH



Recent Literature on MTJ Device
- Choice of Material
- Interface engineering
- Tunneling Between Ferromagnetic materials

Micromagnetic Study of MTJ stack
- LLG Equation for spin Dynamics
- Magnetic Domain Behaviour
- Geometry of MTJ & Thermal Effects
- Different materials and stack configuration

MTJ Mathematical Model
- Static Behaviour
- Dynamic Behaviour
- Bias Voltage Effect
- Temperature Effect
- Stochastic Effect
- Scale Effect

Switching and Device Parameters for different applications

MTJ Stack/Device

Parameter Optimization

Circuit simulation Platform

Compact MTJ Model

MOSFET Model (Industry Std. PDK)

In-Memory Computing circuits

Flowchart for Framework: Device-to-Hybrid MTJ/CMOS Circuit Simulation

Potential Industry Collaboration

- Enterprise Storage
- Automotive
- Aerospace & Defense
- Consumer Electronics
- Robotics and IOT
- AI and Edge computing
- R&D centers

इंडिया सेमीकंडक्टर मिशन
India Semiconductor Mission
Catalyzing India's Semiconductor Ecosystem

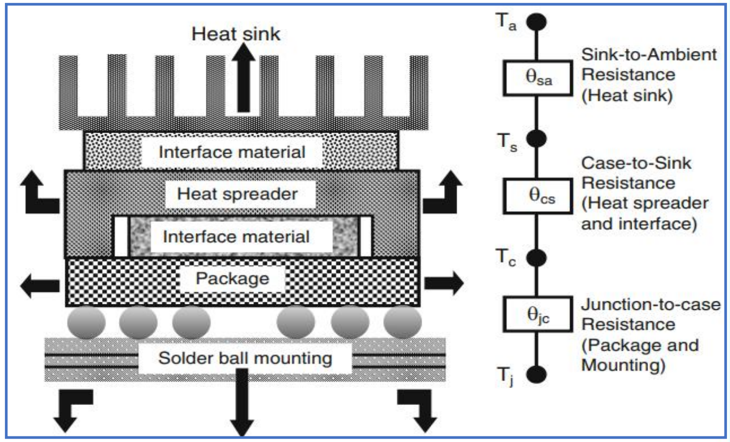
Indian DSPS R&D Team. Together, We Can.

Project 14: Thermal Aware Material Selection and Design-modeling of Advanced IC Packages to Improve Electronics Reliability

Dr. Ribu Mathew, MSIS, MAHE, Manipal, India

Objective:

- Advanced IC packages are complex multi-layered structures realized with different materials and geometry propelled by innovations in material science and fabrication.
- The functionality and reliability of such complex IC packages are an interplay between thermo-electro-mechanical materials, design and process parameters.
- One of the critical failure mechanisms of advanced IC's is temperature induced errors.
- This project aims at developing thermal aware design of advanced IC packages with reduced temperature failures by rational material selection & on-chip design strategies thereby improving electronics reliability.

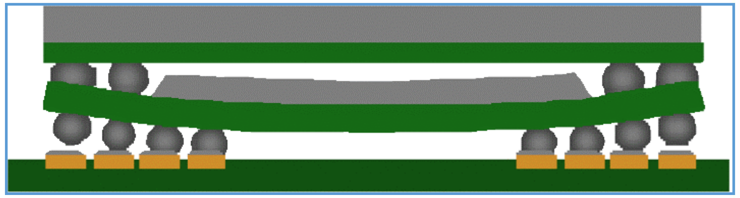


Anatomy of a typical IC package (heat flow)

Entities	Prior art	Proposed
Design domain	Independent material, geometrical and fabrication process choices	Considers the interdependence of material, geometrical and fabrication process
Modeling framework	Focused on performance improvement	Focusses on performance improvement and reliability
Multi-physics	Electrical and mechanical	Thermal, electrical and mechanical & their interdependence
Project focus	Design, modeling & experiment with functionality as focus	Temperature induced failures, & Design of packages to improve electronics reliability

Possible industrial collaboration: IC packaging & EDA companies

Design of experiment:
- Material selection process
- Numerical simulation & FEM
- Validation with experimental results
- Design-Optimization guidelines



Temperature induced failure in a typical package

Parameters under focus:

-Material level (typical material set reported for underfill and other constituent entities): TCE, thermal conductivity, process and process parameters

-Heat generation and dissipation phenomenon- within s/m and to the ambient

-Operating conditions: Electrical, thermal, ambient, packaging levels and tech.

-Dependence on TSV geometry, no. of layers, materials and process

-Reduction in TCE induced wrappage from 100's of microns

References: [1] Kim, H. et.al. 2023. IEEE Transactions on Components, Packaging and Manufacturing Technology.

[2] Lyu, S. et al 2024.. IEEE Transactions on Components, Packaging and Manufacturing Technology.

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Project 15: Disposable Energy Sources for Self-powered Wearable Devices

PI: Dr Amit Kumar Goyal, MIT-MAHE, Manipal - India

Objective: Design, Investigate and Develop a Paper-based disposable power source having V_{oc}>200V, and power>1W/m^2 for self powered wearable devices.

- ☐ Development of disposable power source by considering 2D-material systems.
- ☐ Optimize device parameters to improve the energy efficiency to provide maximum power output with minimal waste.
- ☐ Integration of developed source with wearable device to enhance their lifespan.

Current State of Art: Non-disposable Sources

Device Type	Current state	Applications
Flexible all-printed CS-mode TENG	V_{OC} = 106 V, I_{SC} = 2.4 μA, P=34 mW/m^2	Driving watch and thermometer
Textile-based TENG	V_{OC} = 232 V, I_{SC} = 6.3 μA, 66.13 mW/m^2	Driving a pedometer
Soft textile TENG	V_{OC} = 150 V, I_{SC} = 4 μA, P=393.7 mW/m^2	Power heartbeat meter strap

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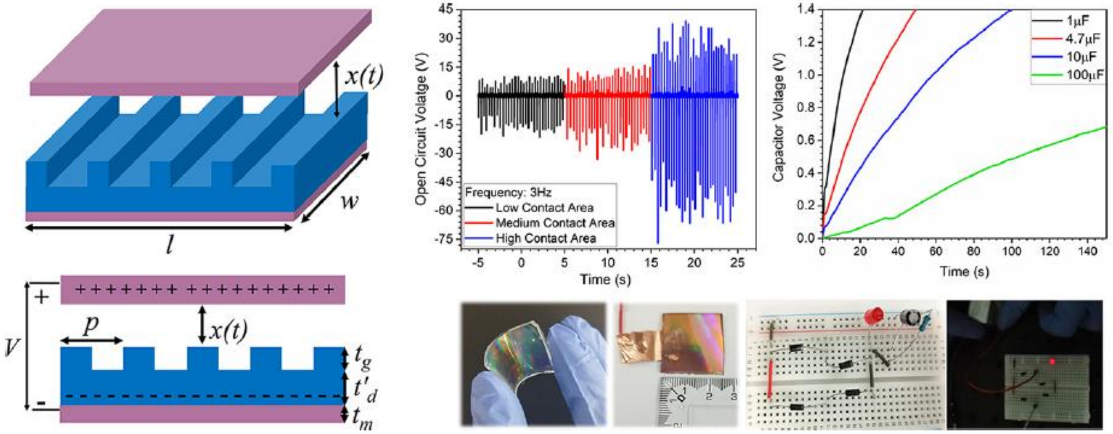
PI Recent Work



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Potential Industry Collaboration

- ❖ Wearable and Print Electronics
- ❖ Portable Electronics
- ❖ Consumer Electronics
- ❖ Point-of-care Devices
- ❖ Energy Management in Smart Cities and Buildings
- ❖ Smart Transports
- ❖ R&D centers

Potential Outcome

- ❖ Compact and Lightweight Design
- ❖ Sustainable Paper-based Device
- ❖ Cost-effective Solutions
- ❖ Eco-Friendly Solutions with Reduced e-waste
- ❖ Improved Wearable Device Lifespan
- ❖ Cleanroom Free Fabrication Process
- ❖ Knowledge Dissemination

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1. Kumar R. et al., "Development of flexible high-performance PDMS-based triboelectric nanogenerator using nanogratings," Journal of Colloid and Interface Science, 669, 458–465, 2024.
2. Xu F et al., "Scalable fabrication of stretchable and washable textile triboelectric nanogenerators as constant power sources for wearable electronics," Nano Energy, 88, 106247, 2021.
3. Pu X et al., "A self-charging power unit by integration of a textile triboelectric nanogenerator and a flexible lithium-ion battery for wearable electronics," Adv Mater, 27, 2472–8, 2015.
4. Liu G et al., "One-stop fabrication of triboelectric nanogenerator based on 3D printing," EcoMat, 3, e12130, 2021.

Project 16 : Design, fabrication and characterization of power inductors on glass substrate packages with high inductance densities and quality factor employing thin film magnetic materials.

Vasu Pulijala, CVN, VNIT Nagpur

Objectives:

- Investigate the magnetic materials for glass substrate embedded power inductors operating in 100-200 MHz range for higher inductance density and quality factors

Approach:

- Explore domain and domain wall engineered thin films of various magnetic materials like NiFe, CoZrTa.

Proposed vs. Prior Art:

	Current Status	Proposed
Inductance density	7 nH/mm^2	>30 nH/mm^2
Frequency range	140 MHz	200 MHz
Quality factor	33 (90 MHz)	>25
L/R$_{dc}$	250 nH/Ω	>1000 nH/Ω
Current density	20 A/mm^2	> 20 A/mm^2

1. Barros, Claudio Alvarez, et al. "Embedded inductors using composite magnetic materials for 12–1-V integrated voltage regulators." *IEEE Transactions on Components, Packaging and Manufacturing Technology* 11.12 (2021): 2183-2192.
2. Bharath, Krishna, et al. "Integrated voltage regulator efficiency improvement using coaxial magnetic composite core inductors." *2021 IEEE 71st Electronic Components and Technology Conference (ECTC)*. IEEE, 2021

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18. Design, fabrication and characterization of high frequency power inductors using magnetic vortex materials

Dr Ashique Ahamed, Dr Murali K P, NIT Calicut

Objectives:

- Investigate the magnetic materials for glass substrate embedded power inductors operating in 200 - 400 MHz range for higher inductance density and quality factors

Approach:

- Explore domain and domain wall engineered thin/thick films of various magnetic materials like FeSiAl, Fe_3O_4

Proposed vs. Prior Art:

	Current Status	Proposed
• **Inductance density**	• 7 nH/mm^2	• >20 nH/mm^2
• **Frequency range**	• 140 MHz	• 200 - 400 MHz
• **Quality factor**	• 33 (90 MHz)	• >25
• **L/R_{dc}**	• 250 nH/Ω	• >1000 nH/Ω
• **Current density**	• 20 A/mm^2	• > 20 A/mm^2

1. Barros, Claudio Alvarez, et al. "Embedded inductors using composite magnetic materials for 12–1-V integrated voltage regulators." *IEEE Transactions on Components, Packaging and Manufacturing Technology* 11.12 (2021): 2183-2192.
2. Bharath, Krishna, et al. "Integrated voltage regulator efficiency improvement using coaxial magnetic composite core inductors." *2021 IEEE 71st Electronic Components and Technology Conference (ECTC)*. IEEE, 2021

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Project 19: Design, fabrication and characterization of super paraelectric (SPE) state thin films on glass substrate with high capacitance densities and quality factor employing MIM geometries and tunable hybrid compounds.

Dr Vinod E Madhavan, Dr Murali K P NIT Calicut

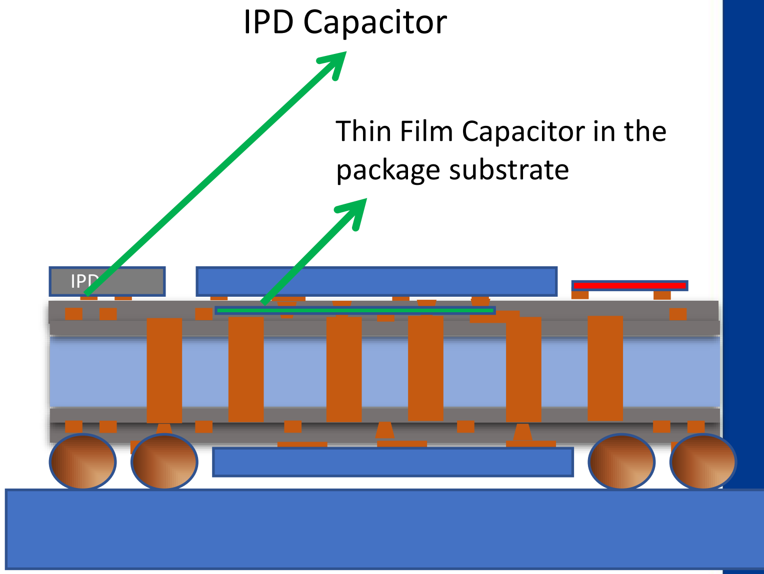
Objectives:

- Investigate the super paraelectric state tuned relaxor ferro electric (RFE) materials for glass substrate embedded capacitors for higher capacitance density and quality factors.

Approach:

- Explore domain and domain wall engineered thin films of various mixture compounds materials like CNF-MIM and RE doped perovskite/relaxor materials

Parameters	***State-of-the-Art***	***Proposed Research Objectives***
Energy Density	• 40 J/cm^3	▪ 100-200 J/cm^3
Efficiency	• 70-80%	▪ 80-98%
Thickness	• > 1 um	▪ 10-100 nm
Leakage Current Reduction %	• < 40%	▪ 40-50%
Dielectric strength	• 1-3 MV/cm	▪ 3-6 MV/cm
TCC		▪ Within 50 ppm/℃



Reference
1. Hao Pan et al. Ultrahigh energy storage in superparaelectric relaxor ferroelectrics.Science374,100-104(2021).DOI:10.1126/science.abi7687
2. Y. Sun et al. Ultrahigh Energy Storage Density in Glassy Ferroelectric Thin Films under Low Electric Field. Adv. Sci. 2022, 9, 2203926. https://doi.org/10.1002/advs.202203926

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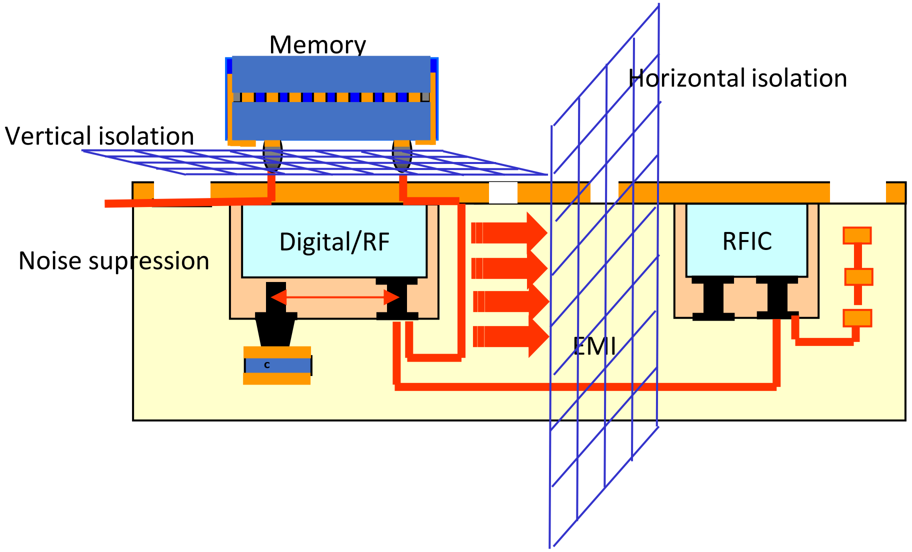
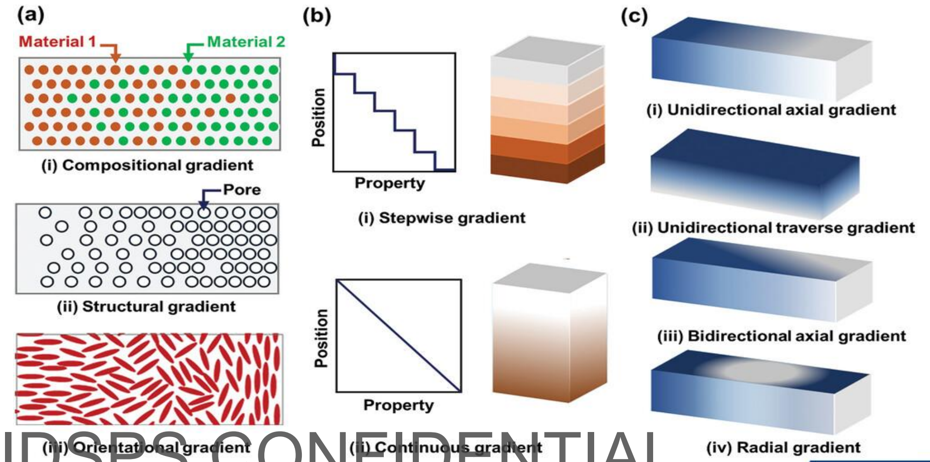
20. Development of EMI shielding in Mixed signal packages - Both for Internal component-component & External package-package isolation

Murali K P , Yogesh N NIT Calicut





FGM structures

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Challenges:

- Existing EBGs require large structures for EMI isolation
- Vertical EMI isolation is difficult to achieve in 3D ICs

Proposed:

- Miniaturized structures with high permittivity, conductivity and permeability materials
- Vertical isolation with novel EMI isolation design and structures

Objective:

MTM superstructure for wide angle and wide band – EHF with RL value ~ -30dB average across the band

Approach:

Functionally Graded Materials

2D magnetic materials

High spin resonance magnetic materials

Layer by layer – absorption/reflection/absorption – better coupling & polarization

Metamaterial Superstructure

References:

1. Xiao-Yun Wang et.al "Electromagnetic interference shielding materials: recent progress, structure design, and future perspective" *J. Mater. Chem. C*, 2022, 10, 4472
2. Ritesh Verma et.al "A review on MXene and its' composites for electromagnetic interference (EMI) shielding applications" Carbon 208 2023 170-190

Thank you!

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