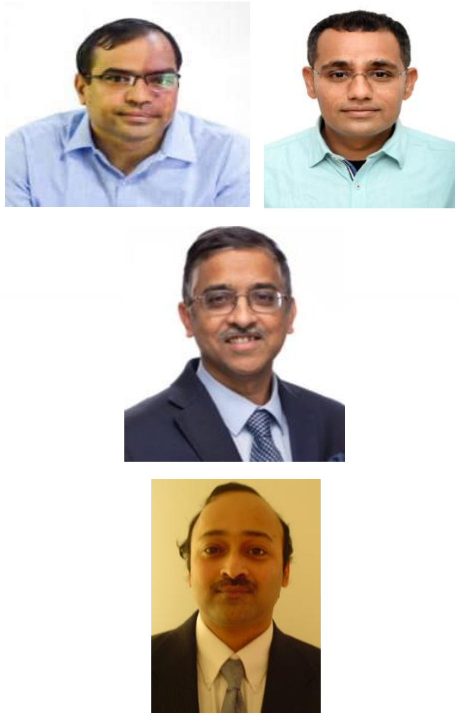
Interconnecting Package Substrates

Industry Co-Development Center (ICC) with Industry Consortium for Next Gen Research, Workforce, and Industry Partnership



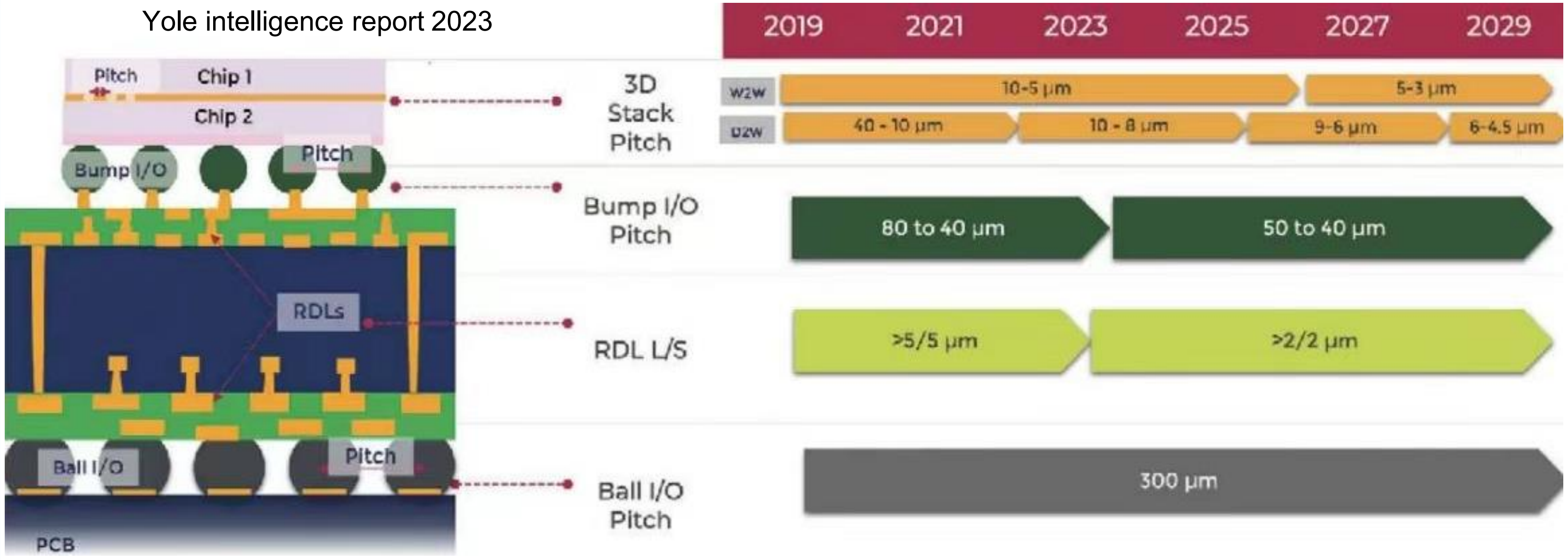
Pradeep Dixit, IIT Bombay (Lead),
Deepak Arora, IIT Jodhpur (Co-lead)

Venky Sundaram, 3D System Scaling (Industry Lead),

Raj Pulugurtha, Florida International University

Next Generation Advanced Substrates : Need & Technical Challenges

Yole intelligence report 2023

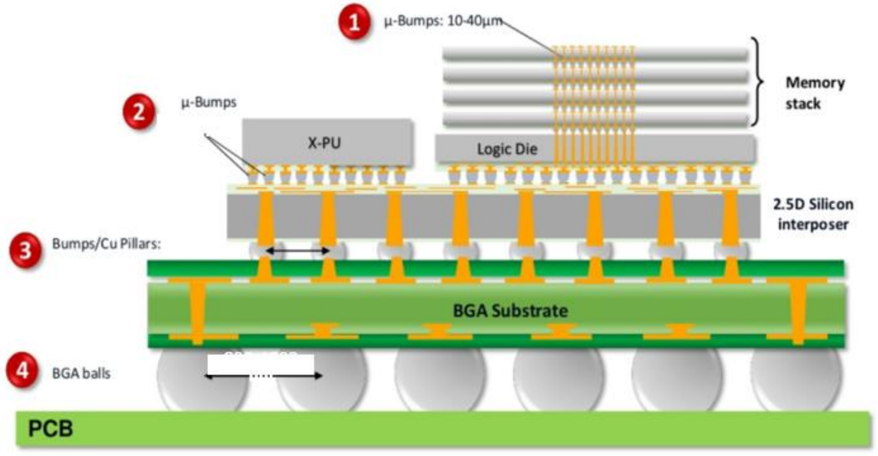


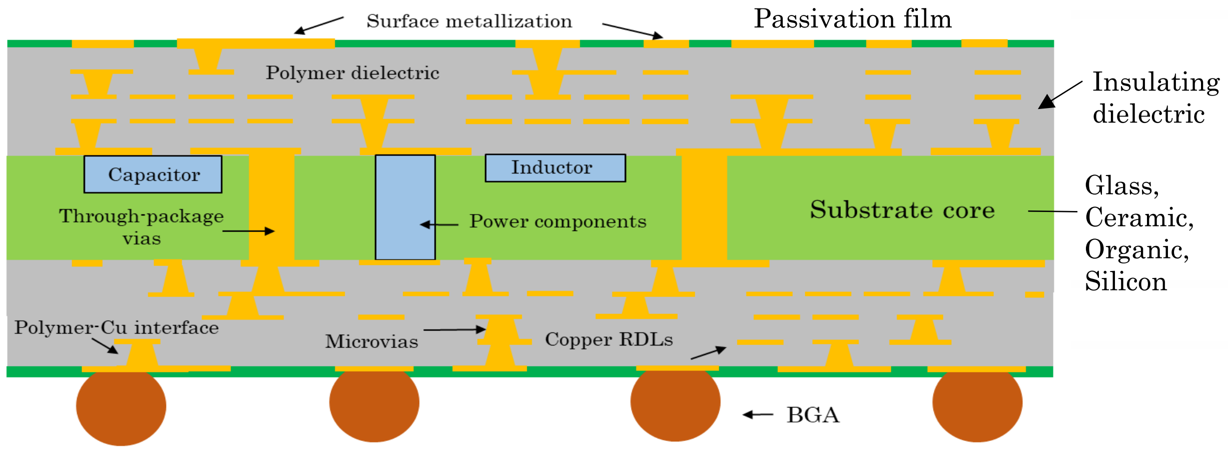
Industry Needs:

- Finer L/S and ultrafine lithography
- Larger substrates
- Substrates for Co-packaged optics
- Glass-based substrates for high-frequency transmission
- Substrates having higher thermal conductivity for high-power electronics

- Technical challenges in the Ultra-High density, Ultra-fine pitch Re-distribution lines (RDL) :
  - Advanced thin polymer dielectrics (< 5 μm) and large-area processing
  - Through via processing (< 10 μm) in polymers / high aspect ratio vias in glass (< 10 μm)
  - Advanced copper electrodeposition: Uniformity (~1%), Smooth surface finish
  - 1 μm lithography: Materials, Tools and Processes

Current State-of-the-art Vs Proposed research





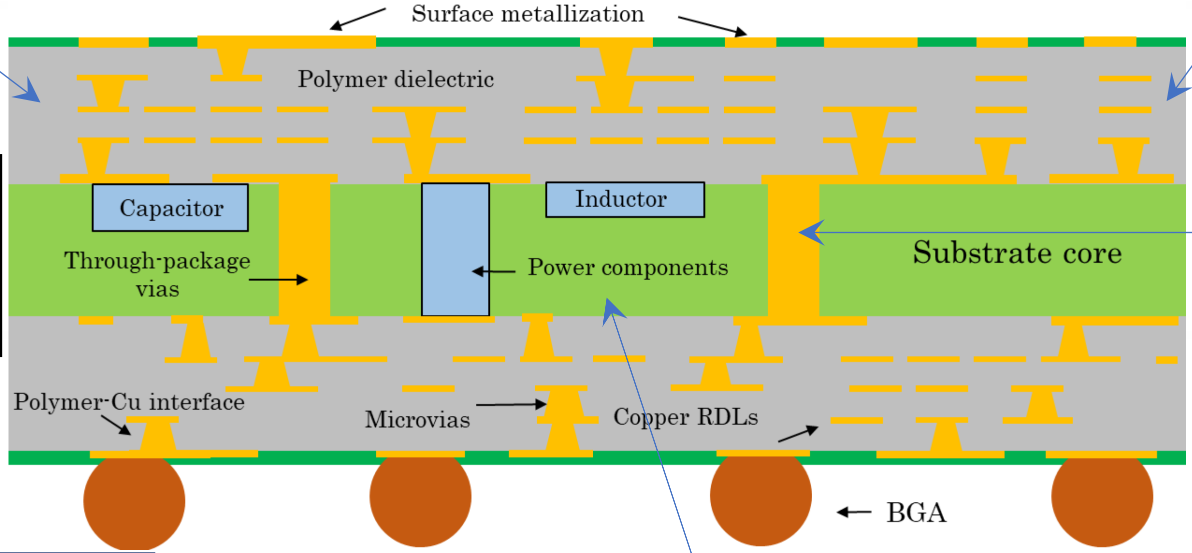
- Redistribution lines:
  - Ultra low-K and Ultra-thin polymeric dielectrics and processes for larger area
  - Ultra-fine (< 5 μm) feature lithography on larger panels
  - Fabrication of Ultra-small micro-vias (<10 μm) in polymer dielectrics
- Substrate core:
  - Faster Through-via formation in glass core and stress-free metallization
  - Embedded components in glass-core package
  - Highly thermal conductive core
- Predictive modelling and Reliability:
  - Predictive modelling and Reliability of TGV and Glass-core packages

Research Vision: Strategic Research Focus Areas and Faculty leads

1. Electrical design for bandwidth and efficient power efficiency
    a) Rohit Sharma, IIT Ropar
    b) Shiv Govind, IIT H

2. Large area lithography materials, processes to achieve 1 μm features
    a) Deepak Arora, IIT J
    b) Nilesh Badwe, IIT K

3. Polymer dielectric materials and processes to create 1 μm RDL
    a) Deepak Arora, IIT J
    b) Pradeep Dixit, IIT B



7. Predictive modeling and design for thermomechanical reliability
    a) Tarun Agarwal, IIT GN
    b) Pradipta Ghosh, IIT GN

4. High aspect ratio Through-Via , metallization, Cavity formation for embedded components
    a) Anurup Dutta, IIT H
    b) Pradeep Dixit, IITB

6. Advances in copper metallization and interlayer adhesion improvement
    a) Pradeep Dixit, IITB
    b) Nilesh Badwe, IIT K

5. Embedded power components
    a) Vasu, VNIT Nagpur
    b) S DuttaGupta, IIT B

Interconnecting Substrates: Multidisciplinary India-wide Faculty Team

Core Faculty Team


Pradeep Dixit (ME, IIT B)
Substrate Fabrication

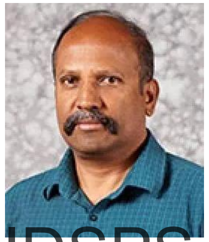

Deepak Arora (CHE, IIT J)
Polymer Processing

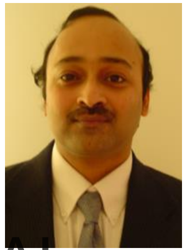

Rohit Sharma (EE, IIT R)
Electrical Design


Nilesh Badwe (MSE, IIT K)
Chip-Board assembly


Anurup Dutta (ME, IIT H)
Laser Processing


Tarun Agarwal (ME, IIT GN)
Predictive Modelling


Mohan Kathaperumal (MSE, GaTech)
Polymer processing, Fine line RDL


Raj Pulugurtha, (MSE FIU)
Embedded components

Cross-SRA Faculty with releveant expertise


Anandaroop Bhattacharya (ME, IIT KGP)
Thermal management


Nilesh Badwe
(MsE, IIT K)
Interconnects


Shiv Govind Singh
(EE, IIT H)
Interconnects


Bhagwati Prasad
(MsE, IISc)
Materials


Shiladri Chakraborty
(EE, IIT B)
Power electronics

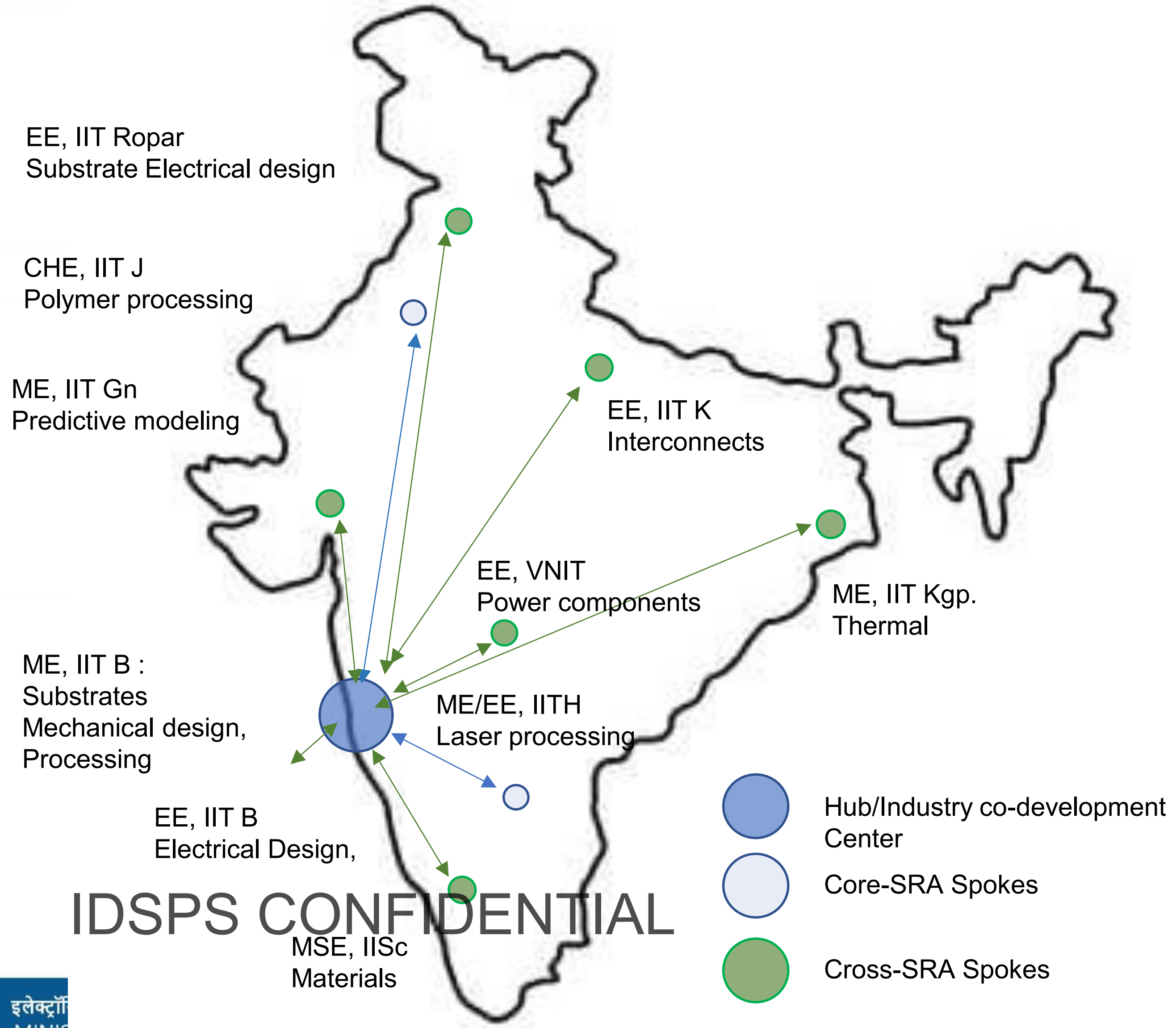

S Duttagupta
(EE, IIT B)
6G Integrated Systems


Mrinal Kant Mandal
(EE, IIT KGP)
6G Integrated Systems


Pradipta Ghosh
(MsE, IIT GN)
Materials Modelling


Poonam Sundariyal
(ME, IIT KGP)
Materials Modelling

Interconnecting Substrates: Hub and Spoke Model



EE, IIT Ropar
Substrate Electrical design

CHE, IIT J
Polymer processing

ME, IIT Gn
Predictive modeling

EE, IIT K
Interconnects

EE, VNIT
Power components

ME, IIT Kgp.
Thermal

ME, IIT B :
Substrates
Mechanical design,
Processing

ME/EE, IITH
Laser processing

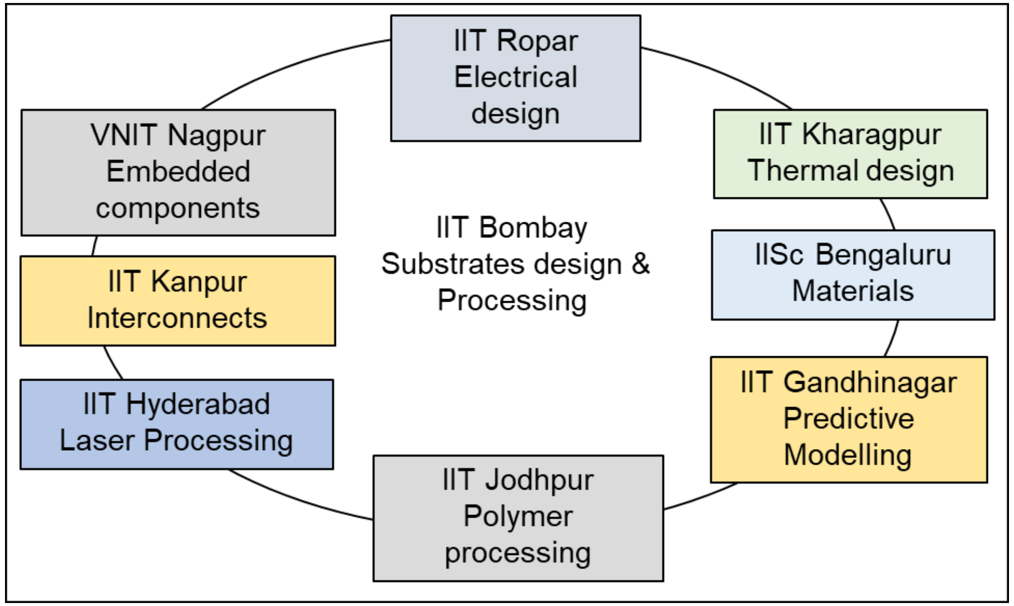
EE, IIT B
Electrical Design,

MSE, IISc
Materials

● Hub/Industry co-development Center

○ Core-SRA Spokes

● Cross-SRA Spokes



IIT Ropar
Electrical
design

VNIT Nagpur
Embedded
components

IIT Kharagpur
Thermal design

IIT Bombay
Substrates design &
Processing

IIT Kanpur
Interconnects

IISc Bengaluru
Materials

IIT Hyderabad
Laser Processing

IIT Gandhinagar
Predictive
Modelling

IIT Jodhpur
Polymer
processing

Technology workforce Development and Education Programs

- Current Courses at IIT B & IIT J:
    - Introduction to Microsystems Packaging
    - Thermal Design of Electronic Equipment
    - Polymer Processing
    - Statistical Process control
- New planned Courses:
    - Electrical design of Substrates
    - Materials for Packaging
    - Electronic Package Design
    - Experimental stress analysis Lab

	5 Years	10 Years
B.Tech	50	100
M.Tech	30	80
Ph.D	10	40

- Planned Lab Courses for UG/PG students:
    - Hands-on training on Electronic Substrate fabrication
        - Organic, Silicon and Glass substrate
    - Hands-on training on the metallization domain
        - Via formation module – DRIE, laser ablation
        - Electroless and Electrolytic plating
    - Masters and PhD students working on industry-relevant challenges
    - Online courses/workshops for working professionals and technicians
        - 1-2 week long certification courses
    - Technicians' training of use of equipment
        - Month-long hands-on training of students at US collaborating institutions through short-term govt.- sponsored student exchange mobility grants
        - Global annual Ph.D. virtual summer school on Electronic Packaging

Target: 1500+ working professionals/ Technicians in the Electronic Substrate domain through short-term seminars and certification in the next year 5 years

List of Potential Industry Partners

Design

- Ansys

Supply chain

- Schott
- Ajinomoto
- 3DGS
- MacDermid Alpha
- Corning
- Growel
- MKS
- Resonac
- CuNex GmbH
- Mitsui
- Baba Fine Chemical

Manufacturing

- Kaynes
- Micron
- Baba Fine Chemicals
- NTK Technologies

Users

- Sandisk
- Infineon
- Micron

IDSPS CONFIDENTIAL

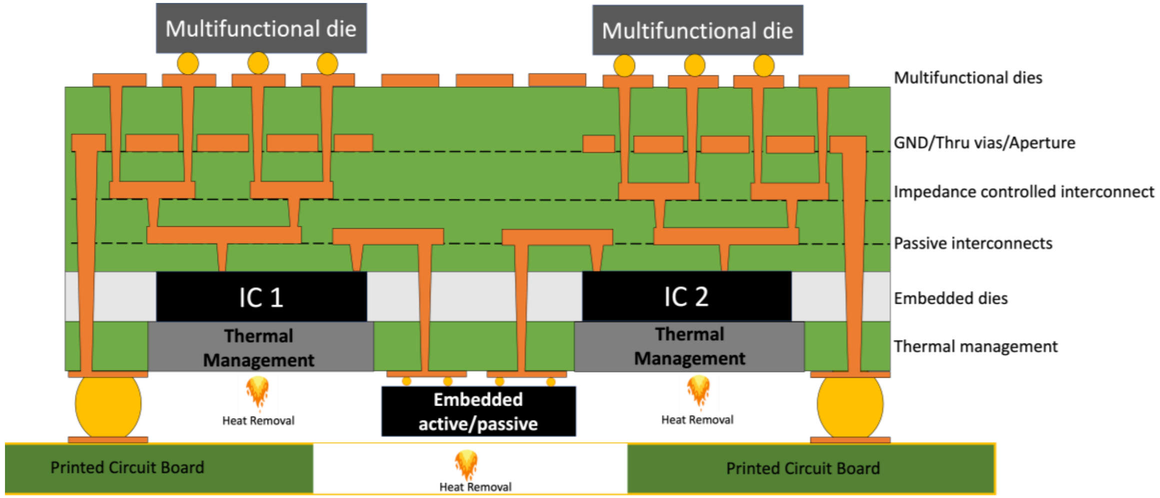
List of Research Projects with Faculty Leads and Institutions

1. Electrical design and performance optimization of low-loss ultra fine-pitch interconnects for next-package substrates
   - Rohit Sharma (IIT Ropar)
2. Polymeric Dielectrics for Build-Up Layers Enabling 1 μm Fine Line Space in HDI Substrates for Large Area Processing (Ajinomoto/ Resonac/ Mitsui)
   - Deepak Arora (IIT Jodhpur), Pradeep Dixit (IIT Bombay)
3. Thin Coreless organic substrate with ultrafine high-density redistribution lines (RDL) (Sandisk / Ajinomoto)
   - Pradeep Dixit (IIT Bombay), Nilesh Badwe (IIT Kanpur)
4. Fabrication of residual-free smaller vias (<10 μm) in polymer dielectric by laser (Schott / Corning)
   - Anurup Dutta (IIT Hyderabad), Shiv Govind Singh (IIT Hyderabad), Pradeep Dixit (IIT Bombay),
5. High aspect ratio through-vias formation by advanced Laser-assisted chemical etching (Schott)
   - Pradeep Dixit (IIT Bombay), Anurup Dutta (IIT H),
6. Electroless copper seed layer directly deposited on glass/silicon substrates (MKS/ Macdermid Alpha)
   - Pradeep Dixit (IIT Bombay), Nilesh Badwe (IIT Kanpur),
7. Next Gen 3D Integration Of Active And Passive Components in the D-band Frequencies (3DGS)
   - Mrinal Kanti Mandal (IIT Kharagpur), Siddhhartha P Duttagupta (IIT Bombay), Raj Pulugurtha (FIU)
8. Integration of Embedded dies in Glass Interposer (3DGS)
   - Pradeep Dixit (IIT Bombay), S. Duttagupta (IIT Bombay)
9. Predictive modelling and design for the Substrate and Interfacial adhesion between copper and polymer dielectrics
   - Nilesh Badwe (IIT Kanpur), Tarun Agarwal (IIT Gandhinagar), Poonam Sundariyal (IIT Kharagpur)

Project 1: Electrical design and performance optimization of low-loss ultra fine-pitch interconnects for next gen package substrates

PI : Rohit Sharma (IIT Ropar)

Objective: This project targets the electrical design and optimization of low-loss fine-pitch interconnects in heterogeneously integrated packages



Die embedded advanced packaging with fine pitch interconnect pathways

Technical challenges:

- High-density, fine-pitch *Cu* interconnects suffer from conductor losses due to surface roughness, process variations and discontinuities
- Significant dielectric loss and thermal impact due to lossy dielectrics at higher frequencies (> 100 GHz)
- Process flow and fabrication is highly iterative due to lack of electrical design of these interconnects

Outcome:

- Machine learning based predictive models for *Cu* interconnects considering TSVs/TGVs, micro vias and solder bumps in glass core substrates
- We propose to reduce the process flow by assessing the impact of surface and dielectric roughness during the initial electrical design cycle
- Electrical-thermal co-design of interconnect pathways considering embedded actives/passives, TSV misalignments and material constraints

	Prior art	Proposed
S21 (on-package)	1.6 dB @ 140 GHz	1 dB @ 140 GHz
S11 (on-package)	< 10 dB @ 140 GHz	< 15 dB @ 140 GHz
Thermal sensitivity study	No	Yes

X. Jia et al., *IEEE Trans. CPMT*, vol. 13, no. 2, pp. 219-229, Feb. 2023

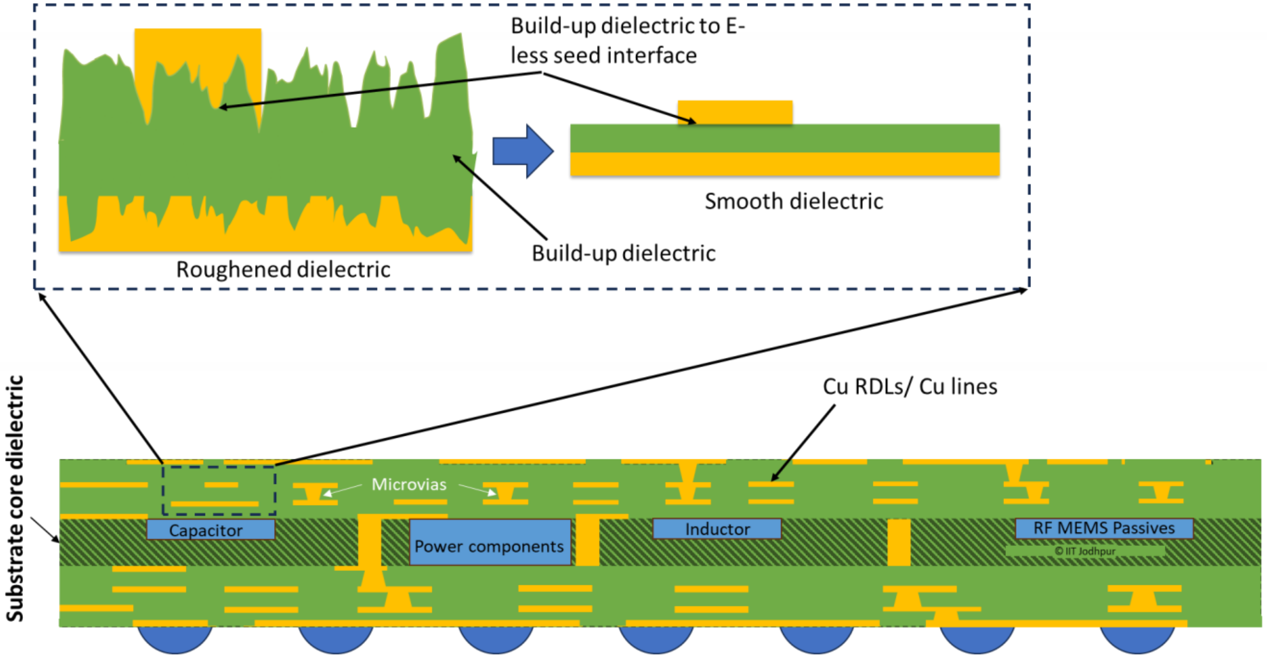
Project 2: Polymeric Dielectrics for Build-Up Layers Enabling 1 μm Fine Line Space in HDI Substrates for Large Area Processing

PI: Deepak Arora (IIT J), Co-PIs: Pradeep Dixit (IIT B)

Objective: Develop polymer materials and processes to achieve 1 μm lithography in about 3 micron thickness with required electrical, mechanical and thermal properties for a 10 layer RDL stack.

Outcome: Prototype demonstrating 1 μm L/S in polymer dielectrics

	Current	Proposed	Drivers
Fine line space (μm)	5 : 5	1: 1	miniaturization
Build up film thickness (μm)	5	3	miniaturization
Build up to E-less seed interface roughness (nm)[2]	300	150	Low transmission loss
Glass transition temperature (T_g) °C[1]	-	230 - 280	Reduced warpage, shrinkage during processing, better handling for large form factors (Reflow temp range ~ 230 – 260 °C)



High density interconnect (HDI) substrate

Saraswati, S., & Arora, D. (2024). Polymer Dielectrics for Electronic Packaging: Curing Dynamics of an Epoxy Resin Blend. 2024 8th IEEE Electron Devices Technology and Manufacturing Conference (EDTM), 1–3. https://doi.org/10.1109/EDTM58488.2024.10512252

Arora, D., Sobieski, D. N., Seneviratne, D., Andideh, E., & Meyer, J. C. (2018). Formation of dielectric with smooth surface (10,070,537). In *US Patent* (10,070,537). USPTO.

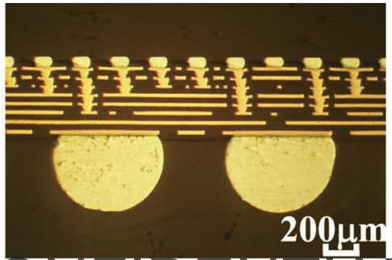
Project 3: Thin Coreless substrate with ultrafine high-density redistribution lines (RDL)

Pradeep Dixit (IIT Bombay), Deepak Arora (IIT Jodhpur)

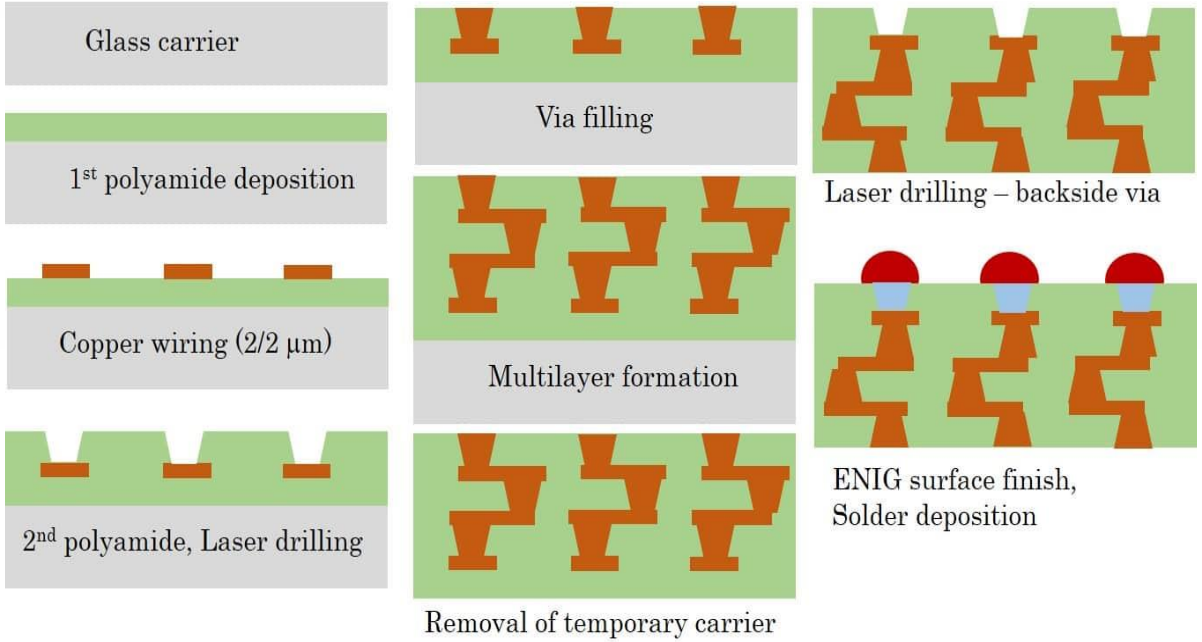
Objective: To develop and demonstrate processes enabling fabrication of thin (< 100 µm) core-less substrate having ultrafine high-density redistribution lines (RDL)

Outcome: Prototype demonstrating a thin core-less substrate (~ 80 µm) having multilayer (>4) ultrafine (< 5 µm) redistribution lines

	Current state	Proposed
Dielectric / thickness	Polyamide/ >10 µm	ABF/ Polyamide/ < 10 µm
Temporary carrier	Silicon/ Glass	Glass
RDL L/S (for coreless)	20 µm/ 20 µm	10 µm/ 10 µm
RDL L/S (for core)	5 µm/ 5 µm	2 µm/ 2 µm
Number of layers	5	> 5
Coreless thickness	> 100 µm	< 50 µm



Approach



Glass carrier

1st polyamide deposition

Copper wiring (2/2 µm)

2nd polyamide, Laser drilling

Via filling

Multilayer formation

Removal of temporary carrier

Laser drilling – backside via

ENIG surface finish, Solder deposition

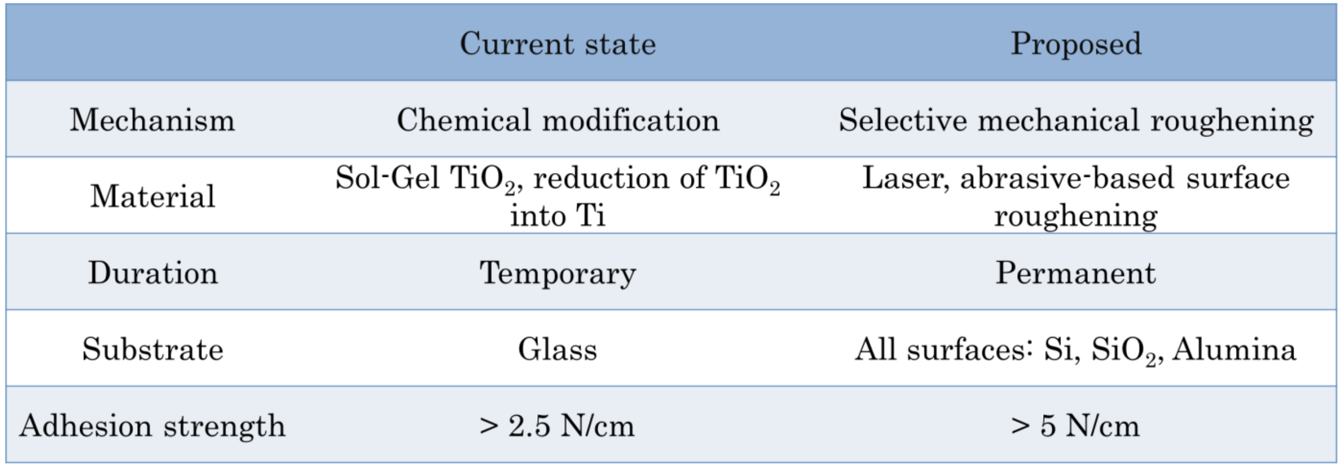
- Islam et al, "High density Ultra-thin organic substrates for advanced Flipchip packages", 69th IEEE ECTC conf. pp. 325 (2019)
- Bonilla et al, "On the path to AI hardware via chiplet integration enabled by high-density organic substrates", 73rd IEEE ECTC, pp. 1374 (2023)

Project 4: Direct deposition of Electroless copper seed layer in high aspect ratio glass/silicon substrates with improved adhesion

Pradeep Dixit (IIT Bombay)

Objective: To develop and demonstrate electroless copper seed layer directly deposited on glass

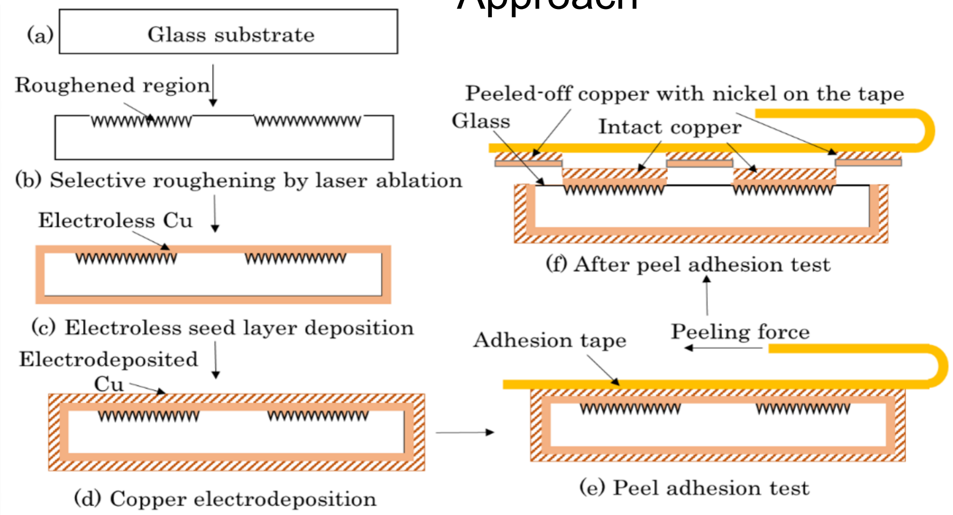
Outcome: Test structure demonstrating direct metallization of electroless seed layer in the through-glass vias (AR > 5).
Peel adhesion strength > 5N/cm

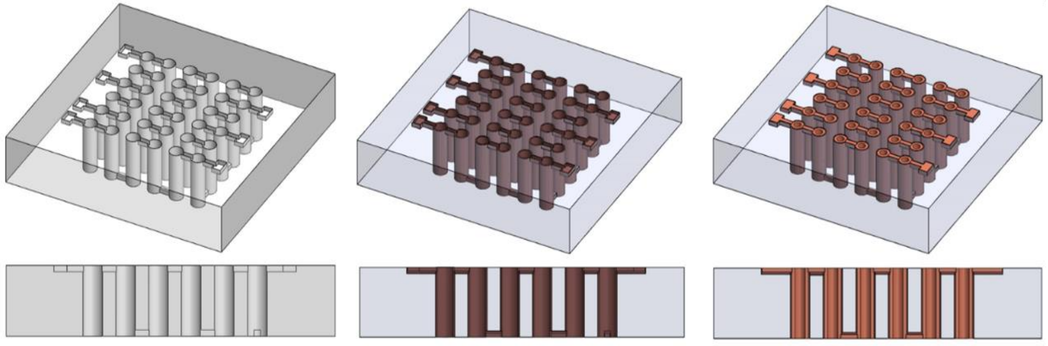


	Current state	Proposed
Mechanism	Chemical modification	Selective mechanical roughening
Material	Sol-Gel TiO_2, reduction of TiO_2 into Ti	Laser, abrasive-based surface roughening
Duration	Temporary	Permanent
Substrate	Glass	All surfaces: Si, SiO_2, Alumina
Adhesion strength	> 2.5 N/cm	> 5 N/cm

- Zawacka et al, "Approaches for a Solely Electroless Metallization of Through-Glass Vias", 72th IEEE ECTC, pp. 889 (2022).
- Pawar et al, "Facilitating electroless metallization of blind holes in glass substrates by electrochemical discharge-assisted surface roughening", Mat. Lett., 358, pp. 135853(2024)

Approach





(a) Vias fabrication (b) Electroless deposition (b) Electrodeposition

Project 5: Formation of high aspect ratio through-glass vias by advanced Laser-assisted chemical etching

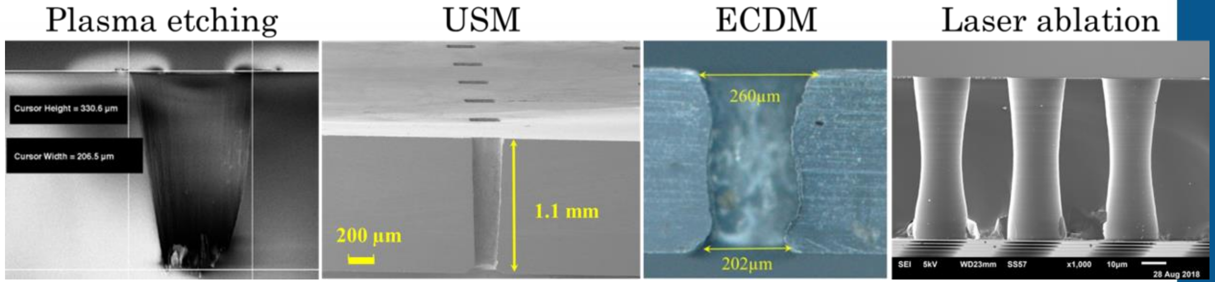
PI: Pradeep Dixit (IIT Bombay), Anurup Dutta(IIT H), Shiv Govind Singh (IIT H)

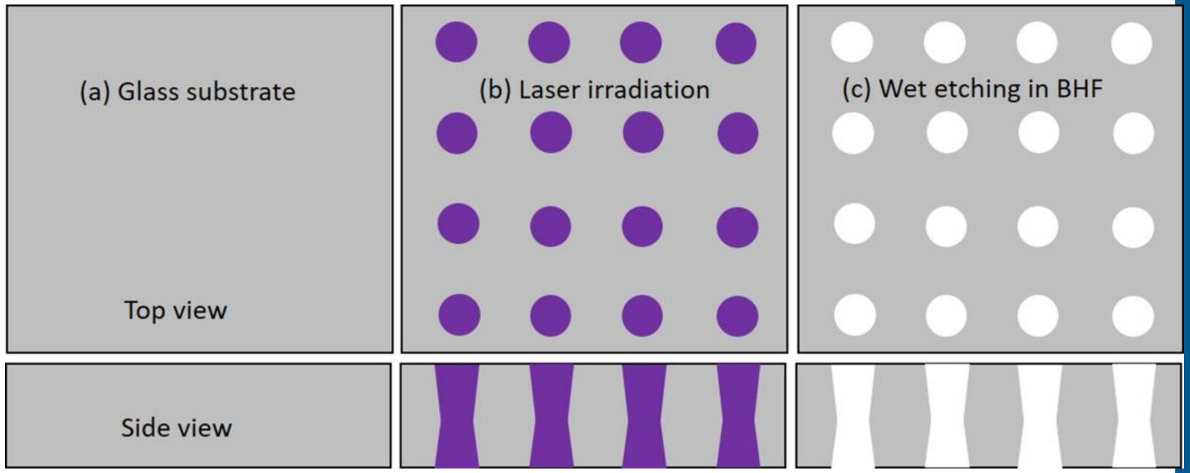
Objective: To develop ultra-fast (~100 μm/min), etching to achieve high aspect ratio (>20) features in glass substrate

Outcome: A prototype demonstrating high aspect ratio (>20) through-glass via formation process, enabling smoother sidewalls without any HAZ

	Current state	Proposed
Mechanism	Laser-ablation	Laser exposure, chemical modification, and wet etching of glass
Etchant	KOH	BHF
Opening size / Aspect ratio	> 10 μm / 10	< 10 μm / 20
Substrate	Glass	All surfaces: Si, SiO_2, Alumina
Sidewall roughness	> 5 nm	< 1 nm

Current vs. Proposed approach





- Kwon et al, "Precise glass microstructuring with laser induced backside wet etching using error-compensating scan path", J. Mat. Process. Tech., 291 pp. 117046 (2021)
- Butkute et al, "Femtosecond Laser Assisted 3D Etching Using Inorganic-Organic Etchant", Materials, 15, pp. 2817 (2022)

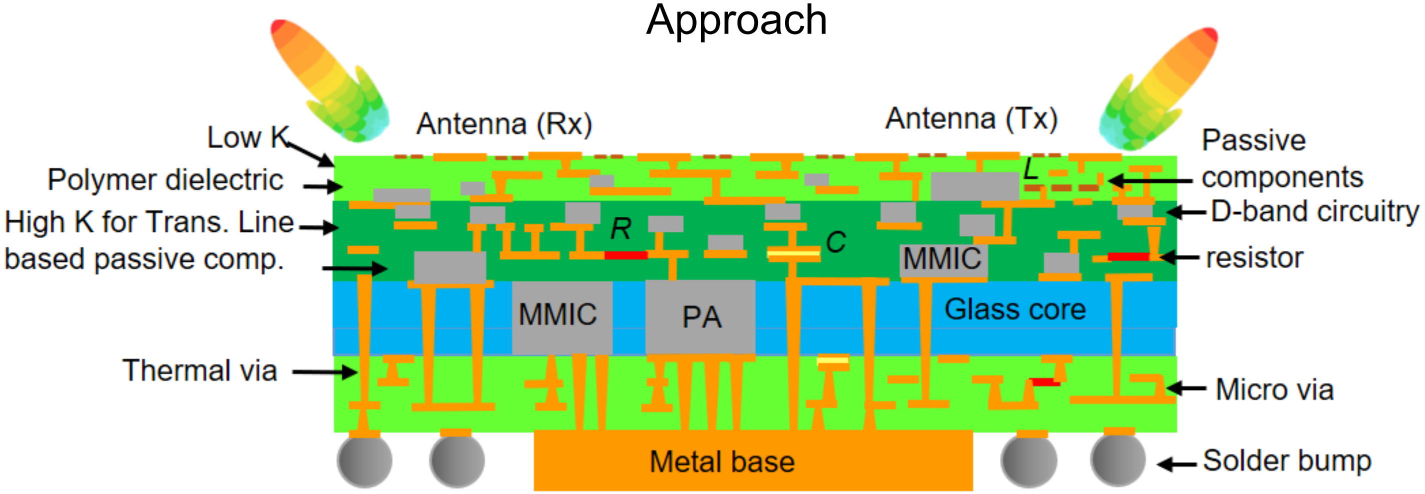
Project 6: Next Gen 3D Integration of Active & Passive Components in the D-band Frequencies

Mrinal Kanti Mandal (IIT Kharagpur), Siddhhartha Prakash Duttgupta (IIT Bombay), Gagan Kumar (IIT Guwahati)

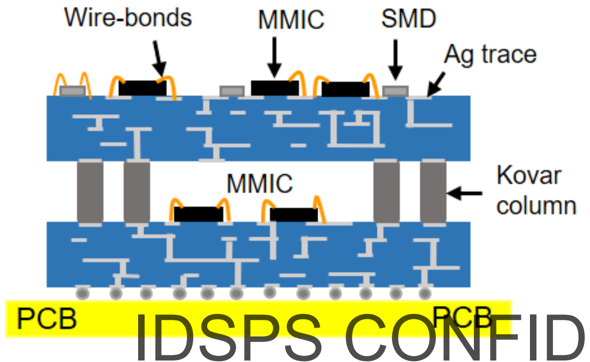
Objectives

- Implementation of a wideband transceiver over 130-150 GHz.
- Use glass core for integrated 3D packaging without any SMD components or wire bonding.
- 3D heterogeneous integration of resistors, inductors, and capacitors along with the chiplets.
- S.I. analysis and cross-talk reduction techniques for D-band high density interconnects. Finding ways to integrate array antennas, RFIC and MMICs in a single package with appropriate parasitic compensation scheme.

Approach



Present



LTCC based packaging: wire-bonds, SMD comp, low density packaging

Proposed

- No SMD comp. or wire-bonds.
- 3d heterogeneous packaging.
- Transmission line based components e.g. power divider, couplers, filters, phase shifter, etc. on a high K material.
- I.L. < 0.5 dB per connection @150 GHz.
- Signal routing density: 2x.

Design and modelling → **Co-design and S.I. analysis** → **Test, characterize, and demonstrate**

References:
1. R. Tummala, and M. Swaminathan, “Introduction to System-on Package: Miniaturization of the Entire System,” Beijing: McGraw-Hill, 2014.
2. Mutee ur Rehman et.al., W-band and D-band Transmission Lines on Glass Based Substrates for Sub-THz Modules, IEEE ECTC, 2020.
3. T. Maiwald et al., Proc. *IEEE*, vol. 111, no. 3, pp. 220-226, March 2023

Project 7: Integration of Embedded Functional dies in Glass Interposer

PI: Pradeep Dixit (IIT Bombay), Siddhartha Duttagupta (IIT Bombay)

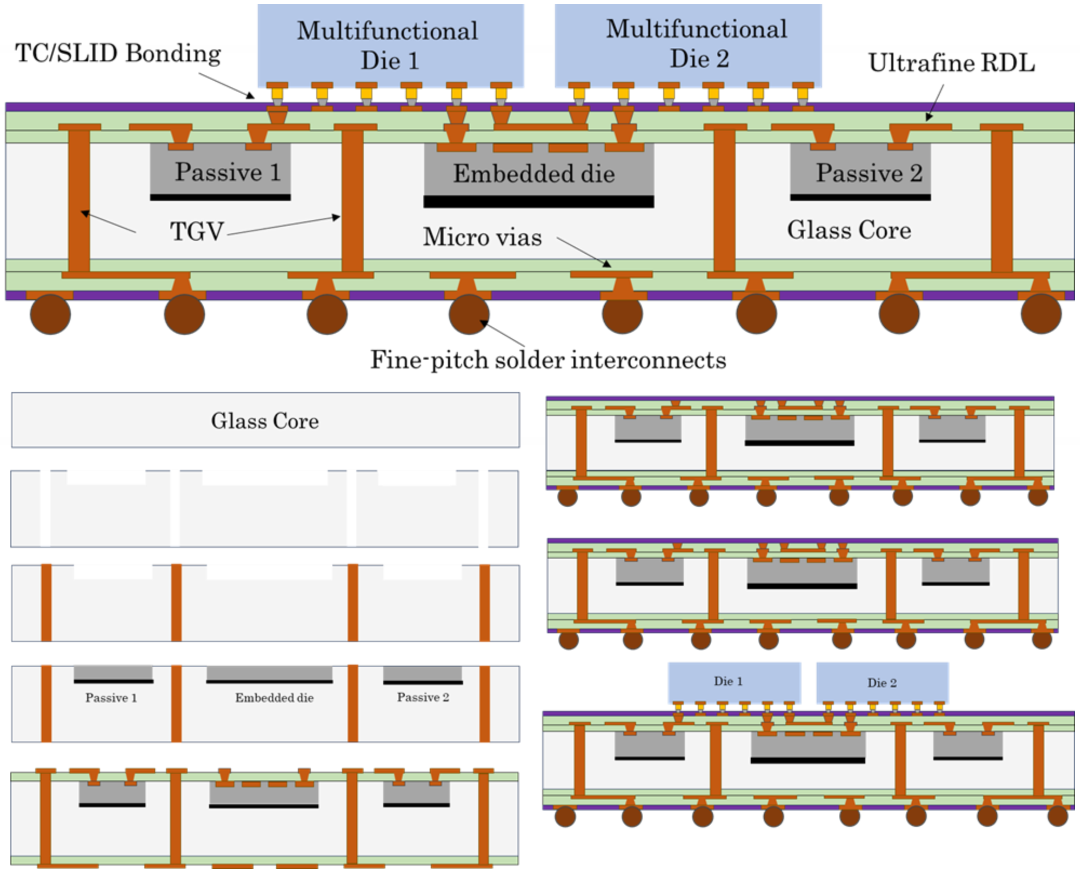
Objective: To develop glass based interposer and embedded dies for ultra-high density advanced packaging

Outcome: A prototype demonstrating glass-core based
interposer having ultra-fine pitch RDLs and
embedded passive components

	Current state	Proposed
TGV formation	Laser-ablation	Laser-assisted chemical etching
Dielectric	Polymer	Glass
Opening size / Aspect ratio	> 10 µm / 10	< 10 µm / 20
Substrate / thickness	Glass / > 300 µm	Glass / < 200 µm
Embedded dies/ Interposer	Yes / Passive	Yes / Active

- Pruek et al, “Glass Interposer Integration of Logic and Memory Chiplets:
- PPA and Power/Signal Integrity Benefits”, 60th IEEE IEEE Design Automation Conference, (2023)
- Ravichandran et al, "Large-body-sized Glass-based Active Interposer for High-Performance Computing", 70th IEEE ECTC, pp. 879 (2020)

Test Vehicle and Approach



Project 8: Predictive modeling and design for Interfacial adhesion between copper and epoxy dielectrics

Nilesh Badwe (IITK), Poonam Sundriyal (IIT Kharagpur)

Objective: To understand the effect of mode mixity (level of mode I vs mode II stress) and defects on the interfacial fracture toughness/strain energy release rate for Copper/Epoxy interface

Prior Art:

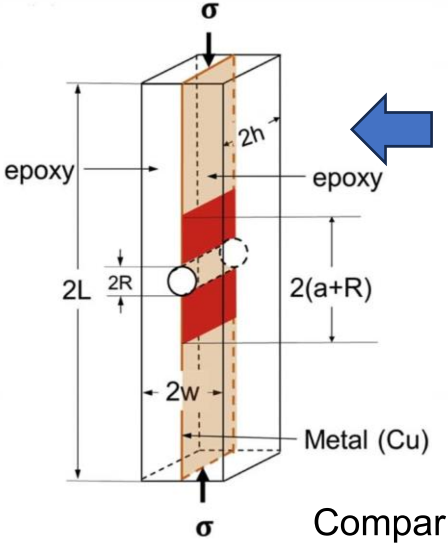
- Common techniques to assess adhesion include:
  - Double cantilever beam (DCB), Peel test, Button shear test
- DCDC specimen used by Badwe et al. has stable crack growth
  - Observed a very small amount concentration of defects (0.5%) can reduce the fracture energy significantly

Technical Challenges:

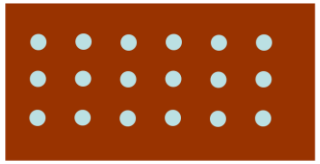
- Interfacial stress → seldom purely mode I (opening) or mode II (sliding)
- Crack length measurement for opaque epoxies may need advanced techniques like acoustic microscopes
- Precise control of defects at the interface and modeling their behavior with respect to the crack propagation
- Identify and model the effect of defect size, pitch, and overall defect density on the strength of a copper/epoxy interface

- N. Badwe et al., Acta Materialia, vol. 103, pp. 512-518, (2016)

Approach



Changing the location of the hole in the centre can change the mode mixity of the stress at the crack tip for the DCDC specimen,



An array of artificial defects will be introduced to study the impact of defect density, size and pitch on the interfacial fracture toughness.

Comparison of Proposed vs. Prior Art

	Current			**Proposed**
Parameters	Peel test	DCB	Button shear	DCDC
Mode mixity	No	Limited	No	Large range
Quantitative	Semi	Yes	Semi	Yes
Stable crack growth	No	No	No	Yes