Integrated Optoelectronics

Industry Co-development Centre with Industry Consortium for Next-gen Research and Workforce

Naresh Emani, IIT Hyderabad **(Lead)**

Sudharsanan Srinivasan, IIT Madras **(Co-lead)**

&

Dr. Ankur Aggarwal, Celestial AI (**Industry Lead**)

&

Global academic collaborator

Prof. Ajey Jacobs, Univ. of Southern California, U.S.A

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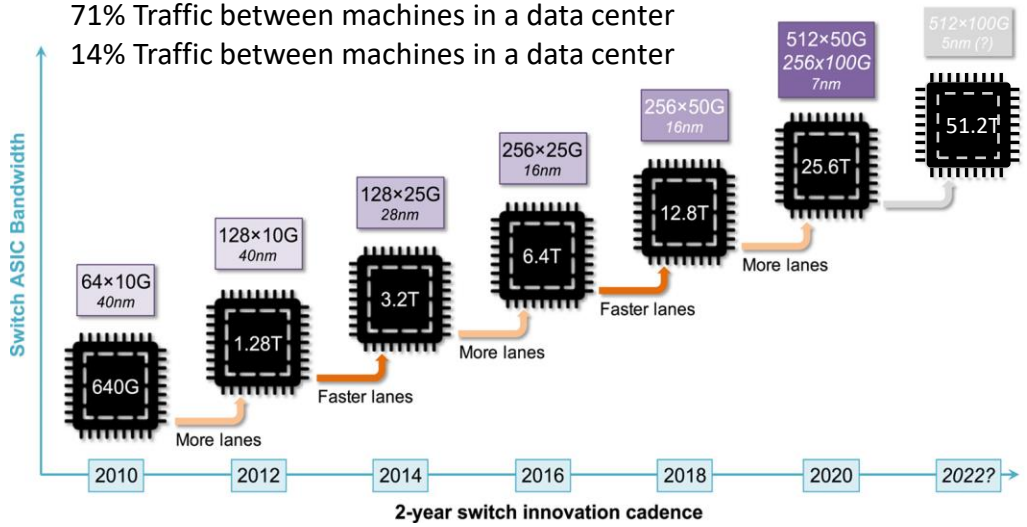
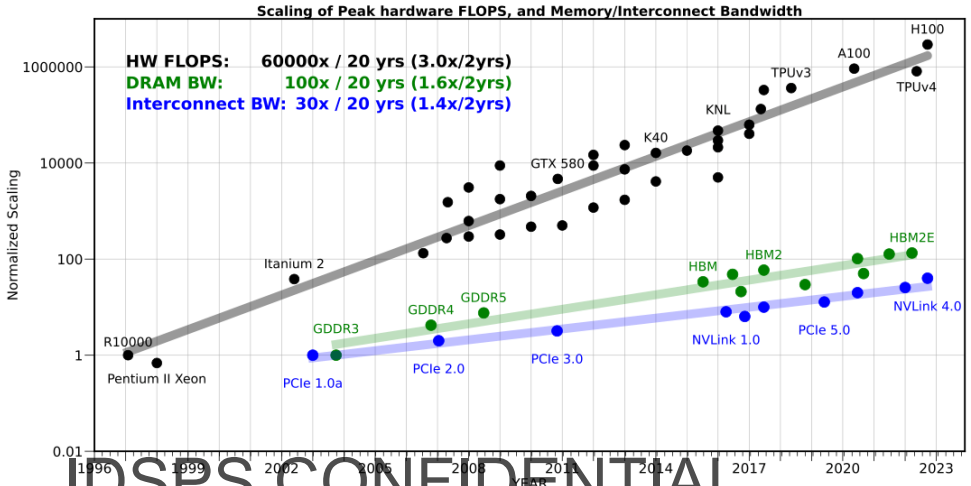
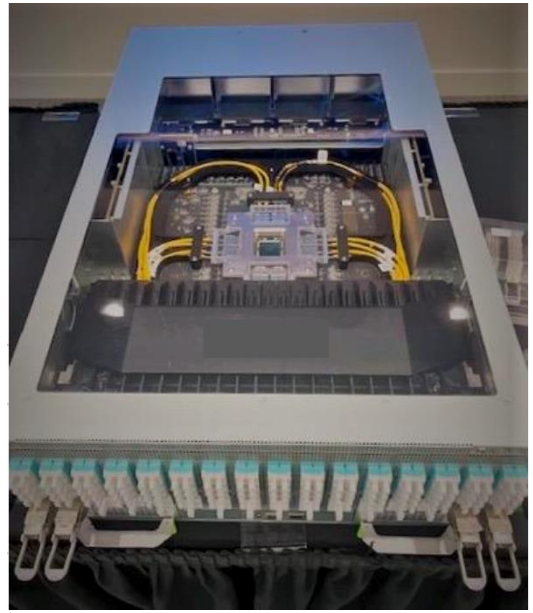
Next-Gen Industry Needs and Technical Challenges

71% Traffic between machines in a data center
14% Traffic between machines in a data center







Challenges: Power for off-chip IO and IO density

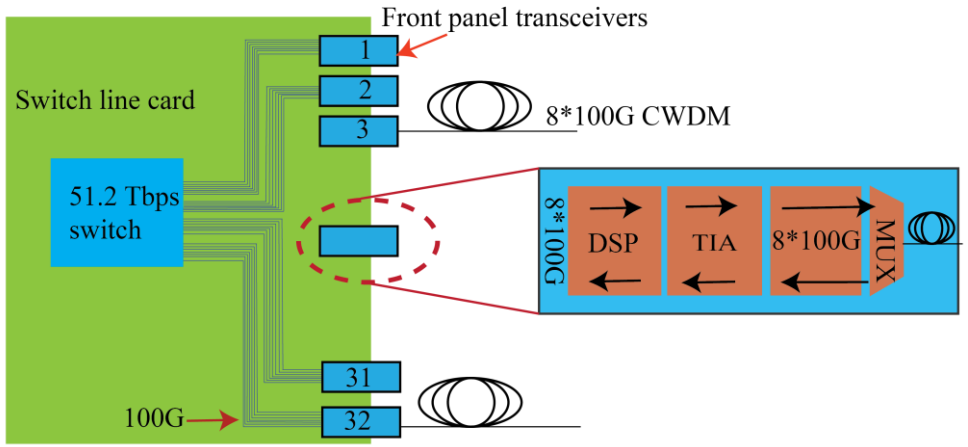
Total CPO revenue expected to grow from **$95 Million[2025]** to **$1.2 billion[2035]**, CAGR ~ 30%, source: IDTechEx Research

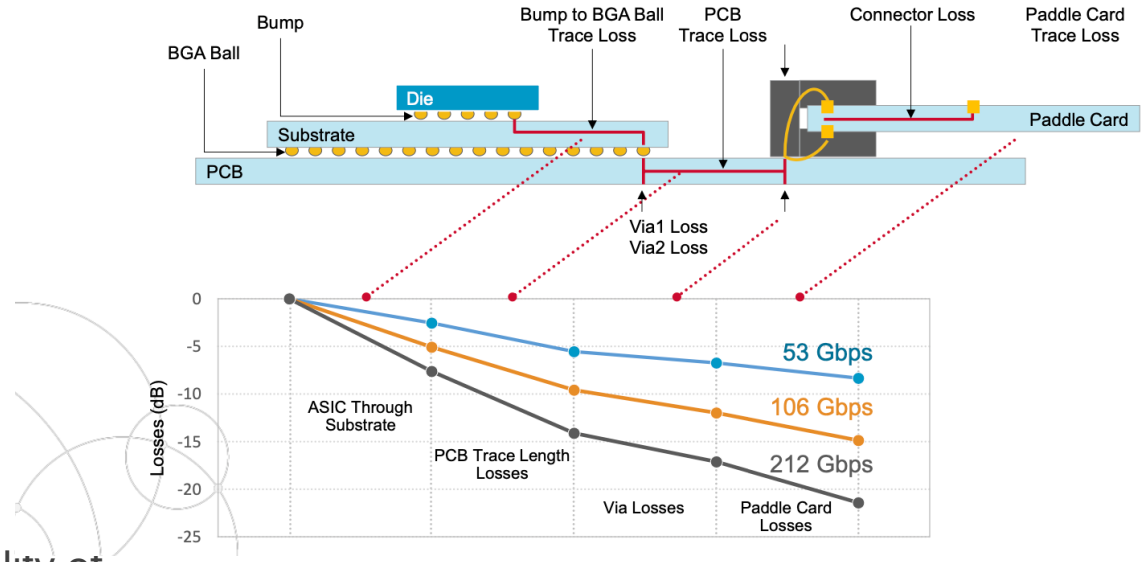
https://doi.org/10.48550/arXiv.2403.14123

Minkenberg, et. al., IET Optoelectronics, 15(2), 2021.

Technical Challenges in CPO

Technical Challenges: Power for off-chip IO and IO density





❶ Energy per bit of 10 pJ/bit @ 100 Tbps → **1000W power consumption**

❷ DSP needed to correct signal distortions and maintain quality of data transmission

❸ Integration of III-V and Si/SiGe

Space between ASIC and OE/EE **< 50 mm**

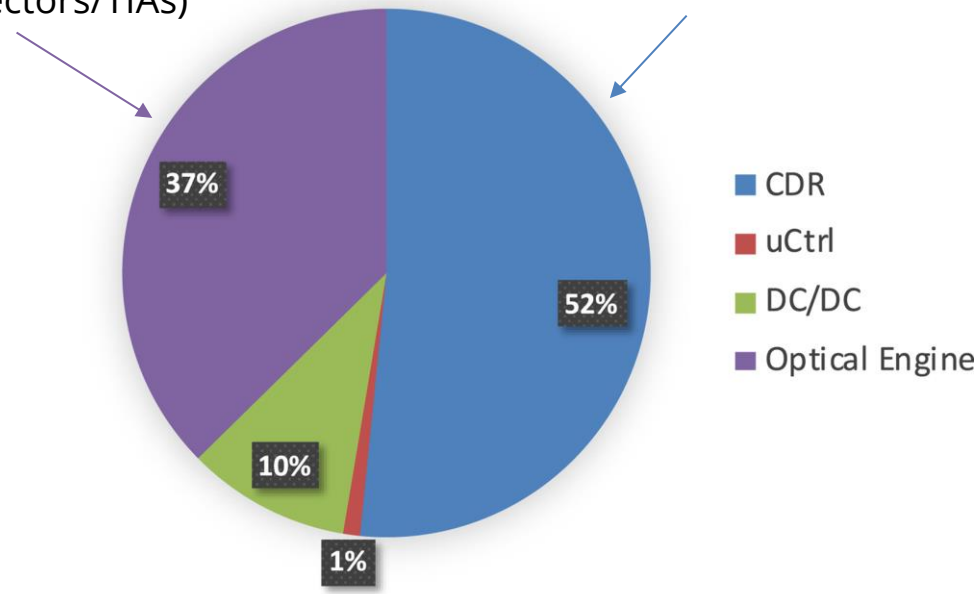
❹ ASIC shoreline IO density **– 500 Gbps/mm**

Minkenberg, et. al., IET Optoelectronics, 15(2), 2021.

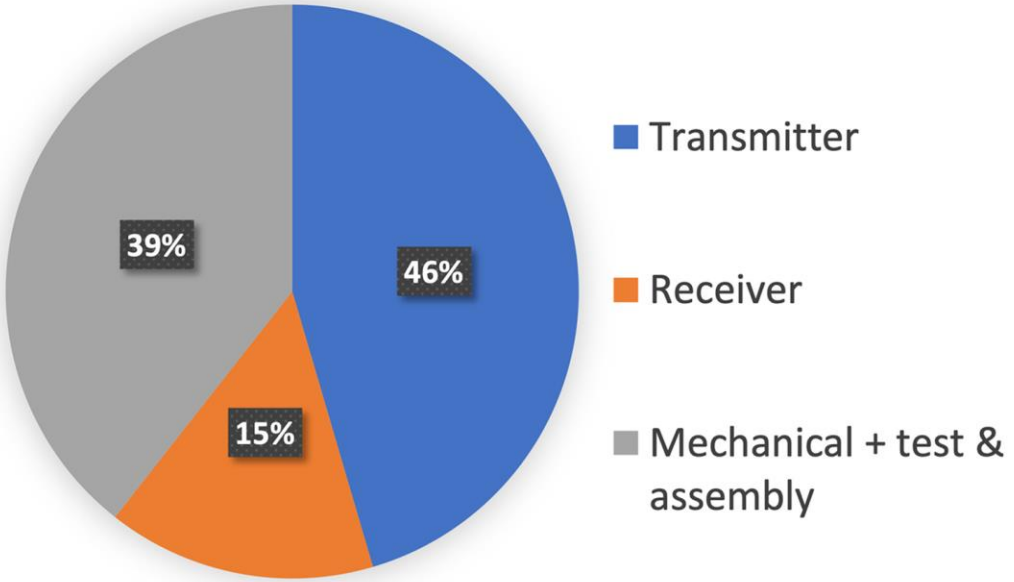
Source: https://www.broadcom.com/blog/accelerating-adoption-of-copackaged-optical-interconnects

CPO – The power and packaging challenges

optical engine (lasers, modulators/ drivers, detectors/TIAs)



Power breakdown of a 400 Gb/s transceiver

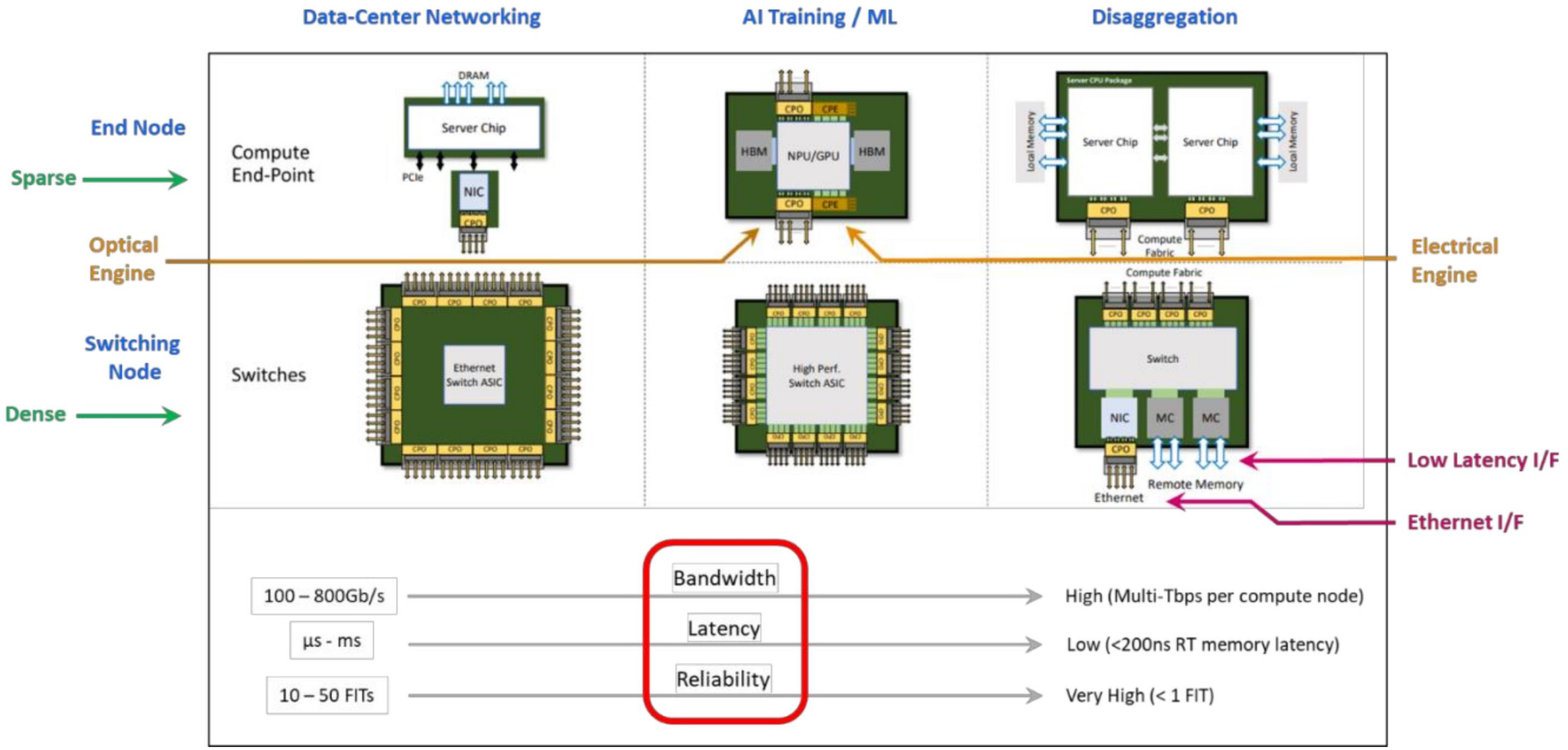


Cost breakdown of a 400 Gb/s transceiver

Reducing power and cost while increasing bandwidth is the key challenge!

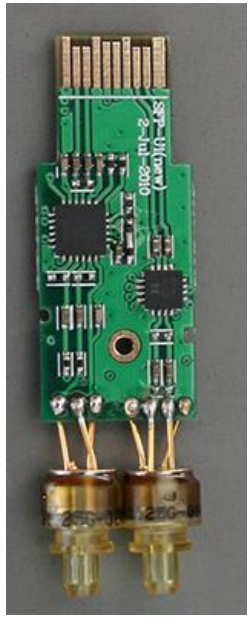
Minkenberg, et. al., IET Optoelectronics, 15(2), 2021.

Other use cases for CPO

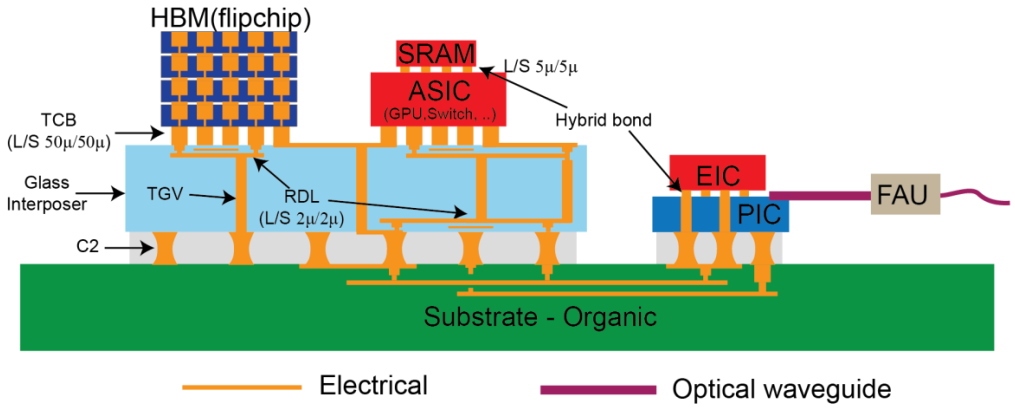


Co-Packaging Framework Document, OIF, 2022

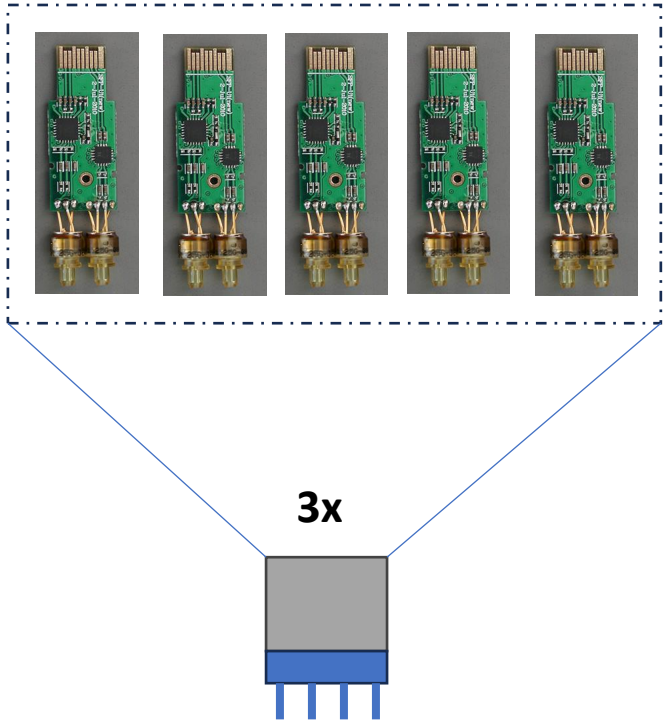
Current and Proposed Approaches



Current



Proposed



CPO Engine

- ☑ Lower **power dissipation** and **higher IO density**
- ☑ Smaller form factor and better reliability
- ☒ Better thermal management needed

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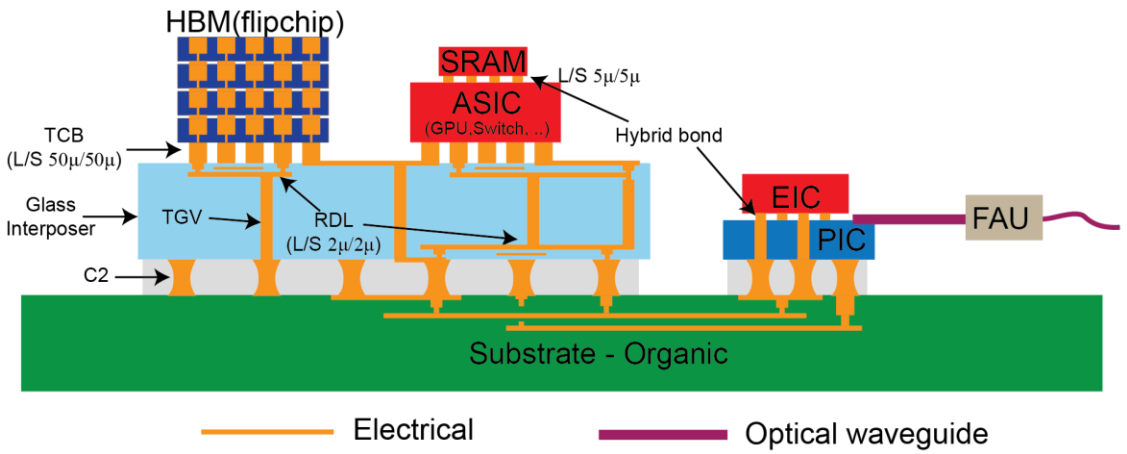
John Lau, Journal of Electronic Packaging, **147** (2025)

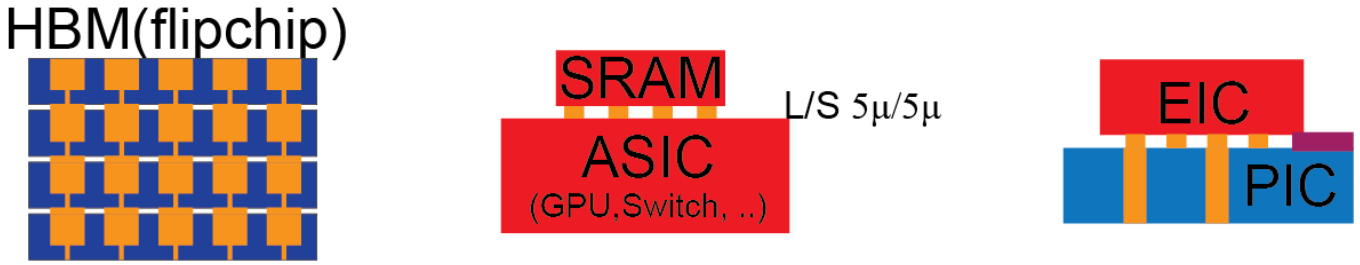
Critical Technologies Needed



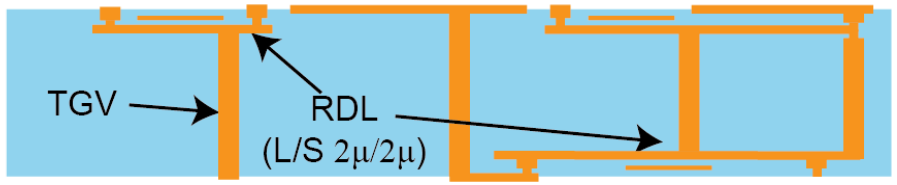
1. Electrical design of a large bandwidth and low power package for AI applications with focus of SI/PI
2. Cu-Cu hybrid bonding of ASIC-SRAM(Si-Si) and EIC-PIC(InP-Si) chiplets
3. Electrical and mechanical design and fabrication of glass interposer with fine pitch RDLs [fabrication @ IITB, substrate SRA]
4. Cu-Cu thermocompression bonding of HBM and ASIC chiplets on glass interposer
5. Assembly on a organic substrate (C2 bonds)
6. Automatic alignment and bonding of fiber arrays
7. Design and fabrication of photonic waveguides in glass

System Integration Approach

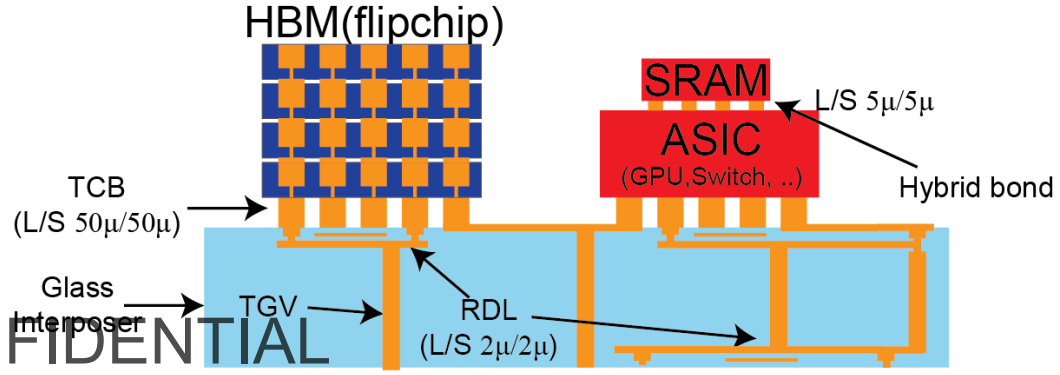
Step 1



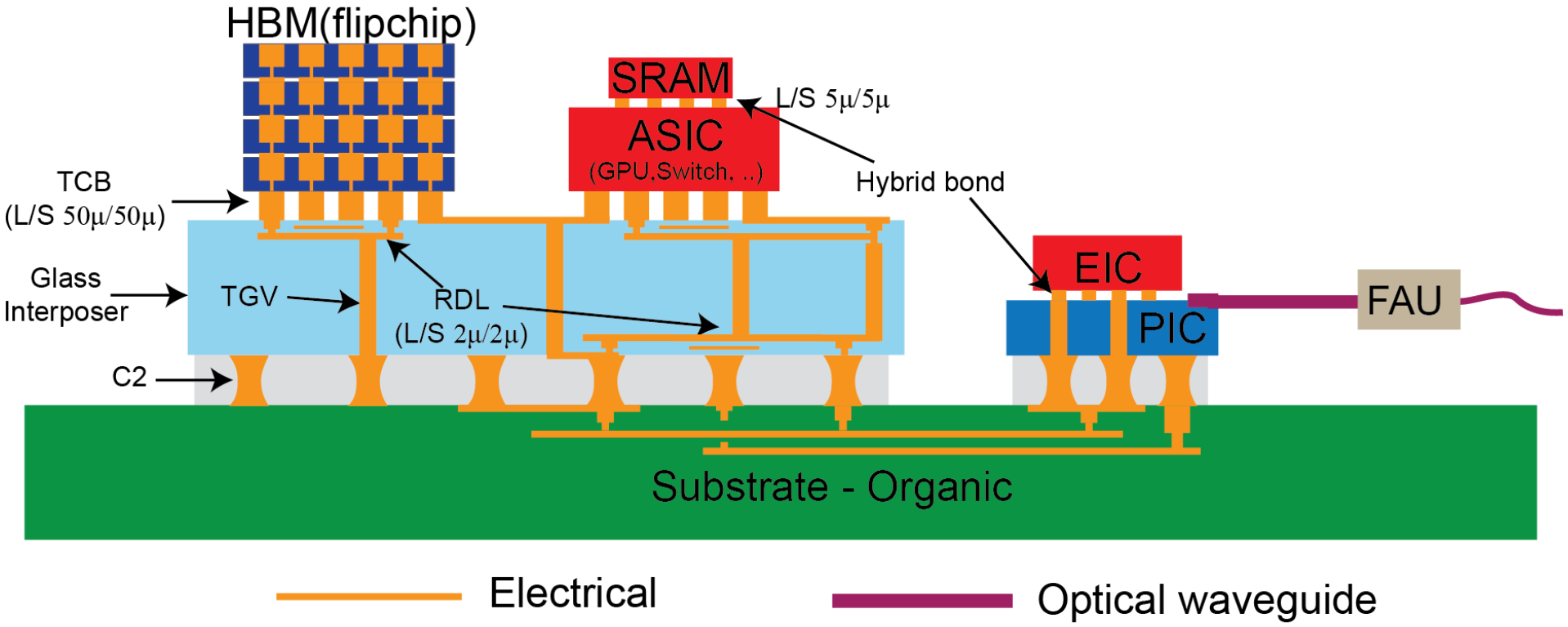
Step 2



Step 3



System Integration Approach



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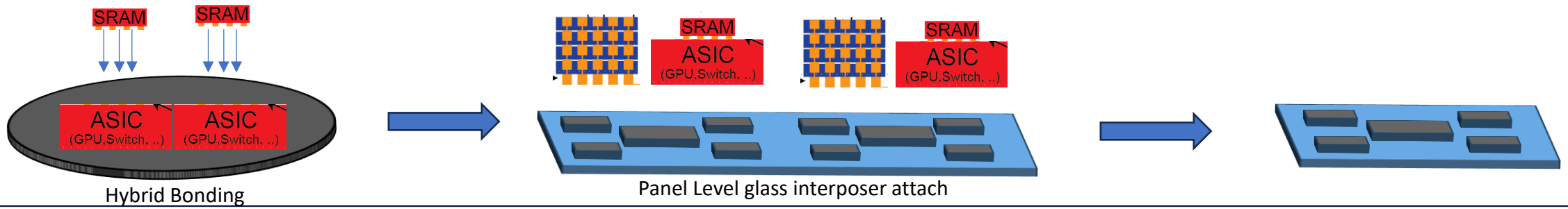
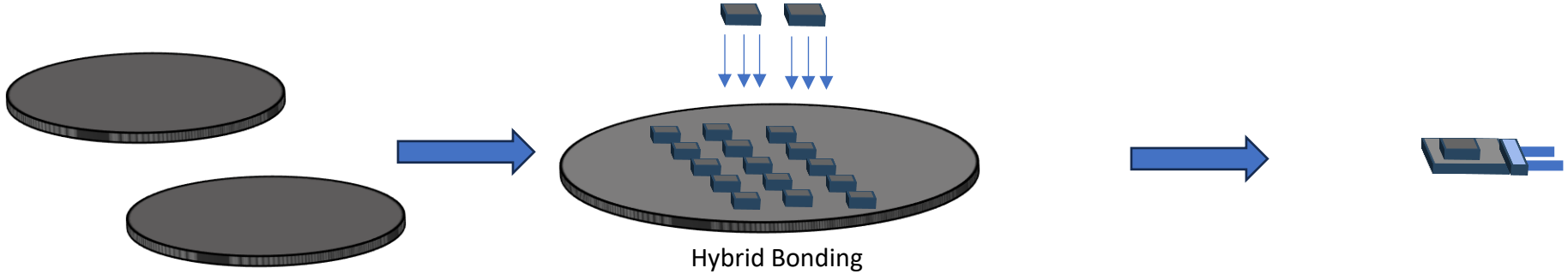
Process Flow

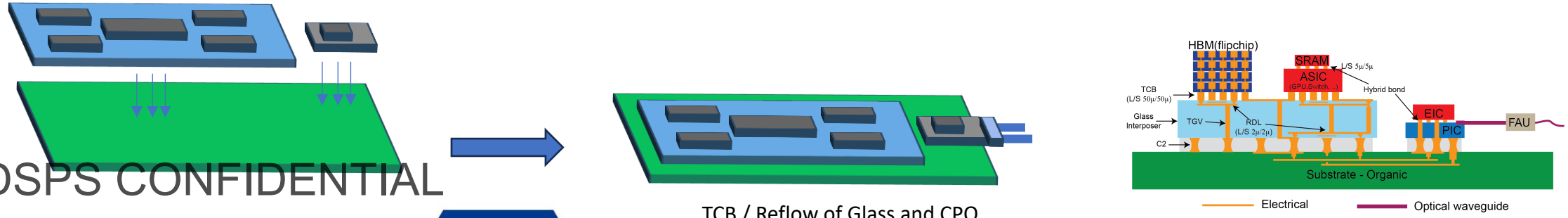
2.5D Integration



3D CPO Engine



2D Substrate Attach



TCB / Reflow of Glass and CPO

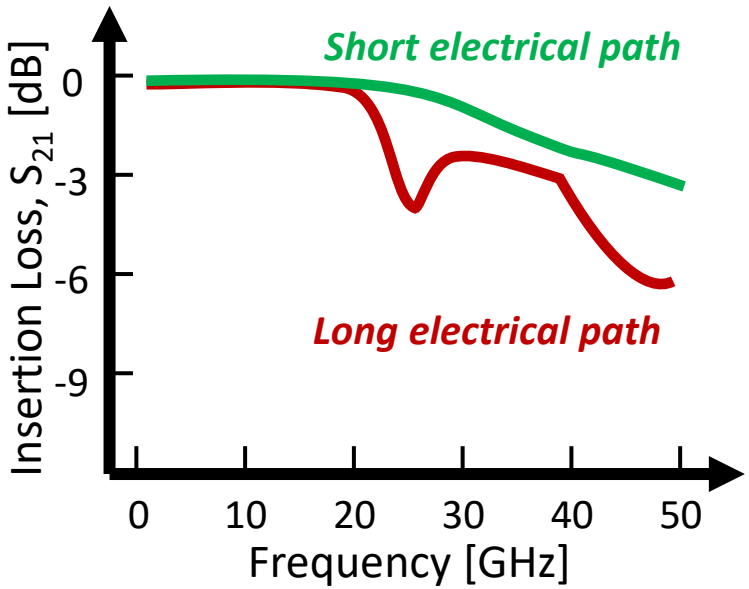
Project 1: Modeling and Co-design of high-speed electronic ICs and photonic transceivers within a single package

PI: Naresh Emani(IITH)

Co-PIs: Sudharsanan Srinivasan (IITM)

Objectives

1. Design electrical and photonic routing on a substrate for low-loss and high-signal integrity
2. Identify designs to bring DSP in the transceiver closer to the network switch
3. To model, design and assess the reliability of the assembled package



	Current state	Proposed
Electrical interconnect length between transceiver and CMOS ASIC	12-15 inch	1 – 2 inch
DSP Power consumption	300-600 W	~50 W
Energy Efficiency	20-25 pJ/bit	~ 5 pJ/bit

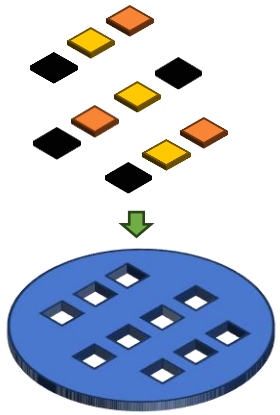
Project 2: Design and Demonstration of optoelectronic integration through multi-die wafer-level packaging

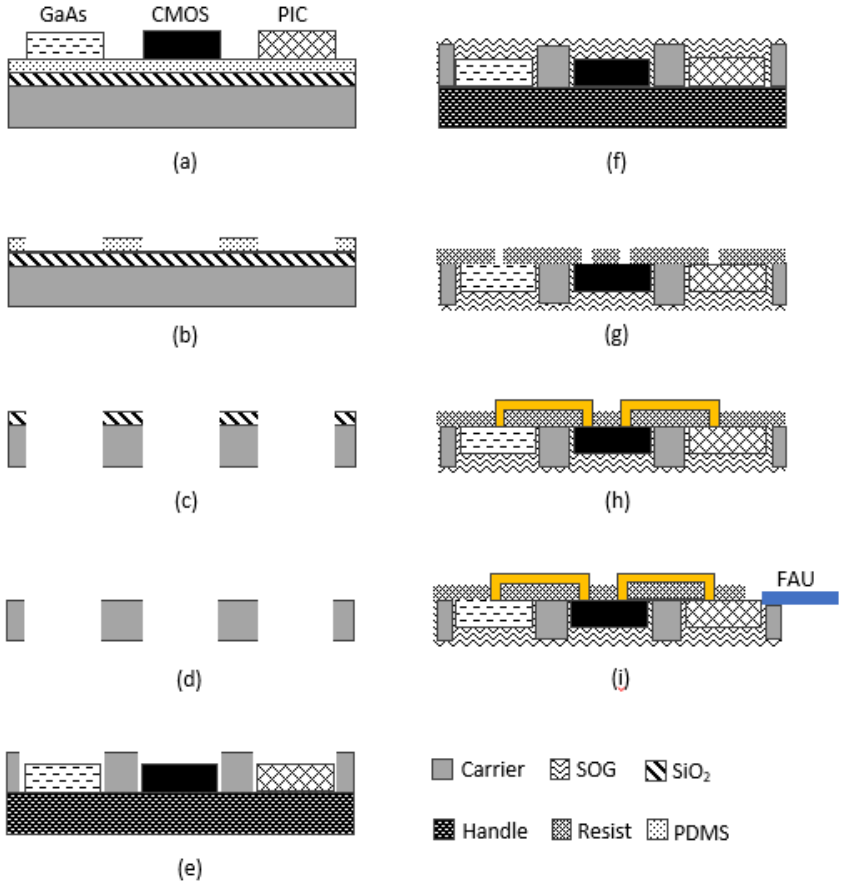
PI: Sudharsanan Srinivasan (IITM)

Objective

Design and Demonstration of optoelectronic integration through multi-die wafer-level packaging

	2.5 D integration (Marvell)	Proposed
Number of connections	10 connections/mm^2	>100 connections/mm^2
Yield	TSV in silicon photonics not mature	High (conventional lithography)
Thermal crosstalk	High (needs calibration)	Small



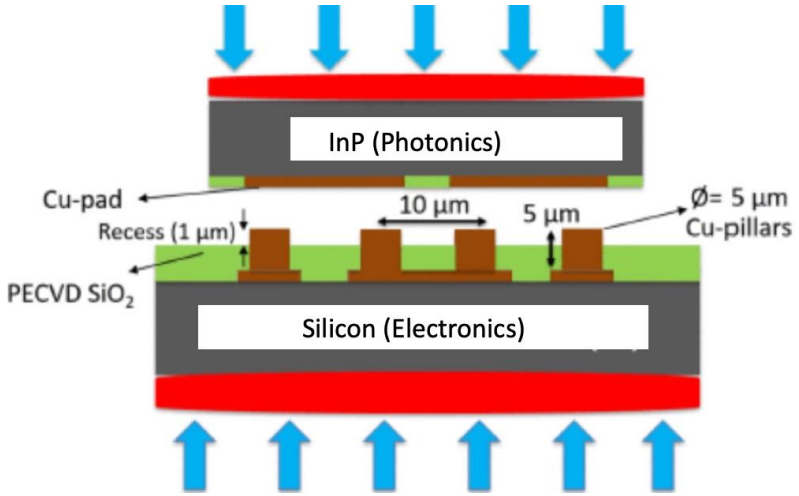


Sodhi et al., Proc. SPIE 8628, Opto. Int. Circuits XV, 86280K (2013)
R. Nagarajan et al., JSTQE, 2023.

Project 3: Cu-Cu Hybrid bonding of InP and Si chiplets on Si and Glass substrate

PI: Shiv Govind Singh (IITH)

Co-PIs: Naresh Emani(IITH), Nilesh Badwe(IITK)



Objective

To develop and demonstrate **low-pressure** and **low-temperature** bonding of InP on Si and Glass

- Challenges: Interface quality, thermal mismatch, InP fragility and bonding interface uniformity
- Surface engineering for preventing surface oxidation of Cu and diffusion of Cu
- Optimization of bonding parameters like annealing temperature, time, pressure, etc. is needed

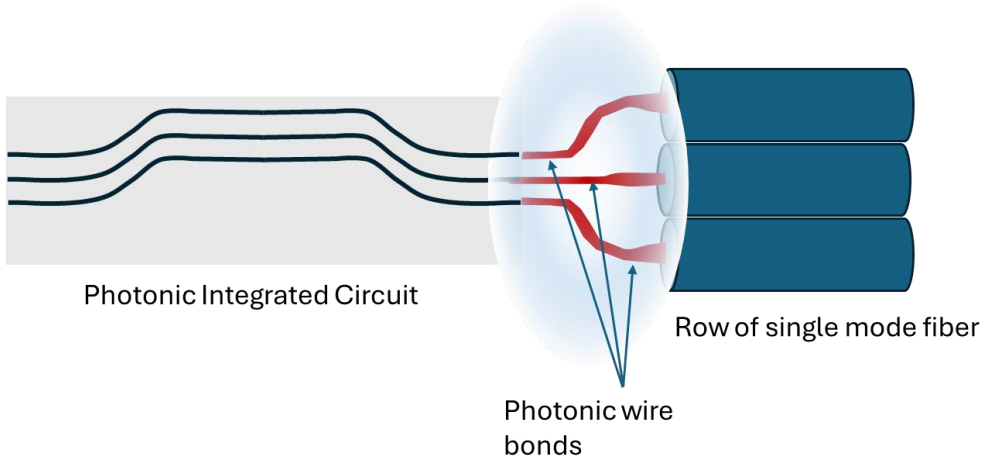
	Current state of the art Si-Si (Cu-Cu)	Proposed InP-Glass/Si (Cu-Cu)
Cu-Cu bonding at InP-Si substrate	<200^{0}C	<200^{0}C
Bond Pressure	<20 M Pascal	<8 M Pascal
Bond strength	>100 M Pascal	>100 M Pascal
Pitch	~20 micron	5-10 micron
Specific Contact Resistance	< 10-7 ohm/cm^2	< 10-7 ohm/cm^2

Project 4 - Automated alignment and bonding of 3D stacked fibers to 2D planar photonic waveguides through ultrafast laser writing

PI: Anurup Datta (IITH)

Objectives

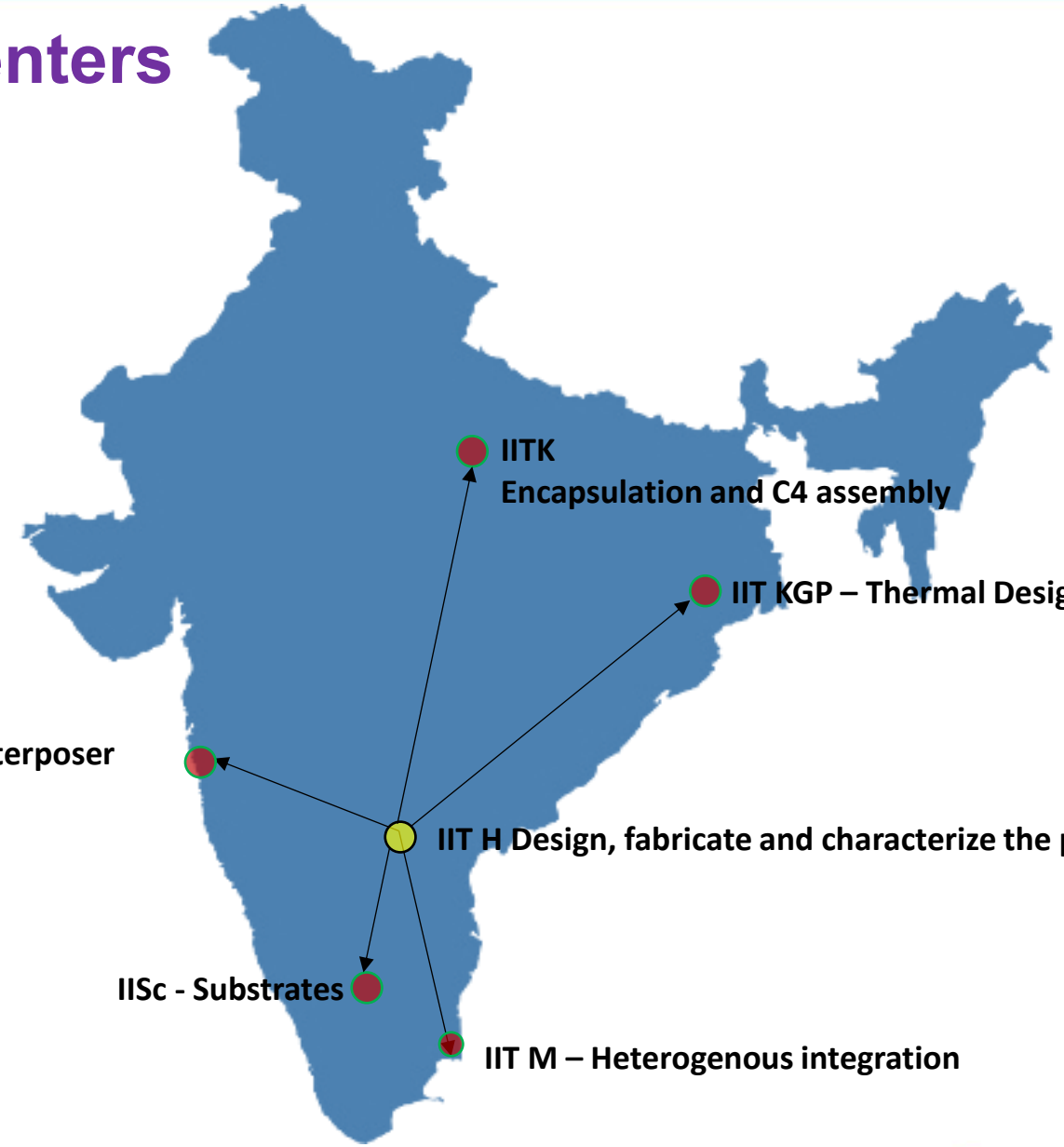
- Develop technologies for in-situ photonic wire bonding through two-photon polymerization
- Increase the shoreline density through photonic wire bonding of 3D stacked fibers to 2D planar PIC waveguides



Proposed vs. Prior Art

	Current state	Proposed
Fiber Array Unit	Single planar array of Fiber	Two layers of Fiber stacked on top of each other
Photonic Wire Bond (PWB) density	40/mm	80/mm
Fabrication time per PWB	30s	30s or better

CPO: Primary & Satellite Centers



Education and workforce development(5 years)

- **Educated workforce target – B.Tech: 75, M.Tech: 50, Ph.D. : 15**
- Offer Electronic Package Design course on NPTEL platform
- Hands-on lab for students/industry professionals on design, assembly, and testing of co-packaged optical devices

Course	BTech	MTech	PhD	Industry/PDC
Introduction to Packaging	☑	☑	☑	
Fundamentals of Electronic Packaging Materials	☑	☑	☑	
Electronic Package Design		☑	☑	☑
Heat transfer in electronic packaging		☑	☑	☑
IC Assembly, Packaging Design and Characterization Lab		☑	☑	
Experimental stress analysis Lab		☑	☑	
Advanced Packaging			☑	☑
Thesis Research		☑	☑	
Industry Internships	☑	☑		

Process Flow with tools needed to build the CPO Prototype

1. Design and simulation of the package prototype

High Performance Computing + EDA tools for electrical and mechanical simulation and modelling (2 Cr)

2. Integration of ASIC-SRAM and EIC-PIC chiplets (hybrid bonding)

- Mask maker (3 Cr)
- Lithography tool (4 Cr)
- Metallization (2 Cr)
- Die bonder with alignment (8 Cr)

3. HBM chiplet integration

- Flip-chip bonder(5 Cr)

4. Glass interposer with fine pitch RDLs

Glass interposer fabrication at IIT Bombay

5. Integration of ASIC-SRAM and HBM chiplets on glass interposer

- Plasma cleaning (1 Cr)
- Thermo-compression bonder (5 Cr)

5. C2 bonding on organic substrate

- Pre-clean
- Solder printing (1 Cr)
- Pick and place tool (2 Cr)
- Curing oven (0.5 Cr)

6. Fiber attach

- Encapsulation and curing oven – 1 Cr
- Alignment optomechanics – 2 Cr
- Glob top dispensing – 1 Cr

7. Metrology and Reliability

- Bond strength analysis - 1.5 Cr
- Electrical characterization(4 Cr)
- NDT (SEM and SAM) – 2 Cr
- IR inspection (5 Cr)
- Thin film thickness measurement – 2 Cr
- AFM – 1 Cr
- Thermal (-40C to 150C) chamber - 2 Cr
- Electromigration setup (4 Cr)
- Vibration tester - 1 Cr
- Optical microscope – 1 Cr
- Drop tester – 1 Cr
- Environment chamber – 1 Cr

8. Optical and electrical Characterization

- Optical and RF probe station – 4 Cr
- SI/PI measurement – 10 Cr
- Optical instrumentation (TLS, OSA, Lightwave analyzer) – 8 Cr

9. Common infrastructure and additional tools

- Cleanroom – 10 Cr
- BTech/MTech Teaching Lab infrastructure – 3 Cr
- Wire bonder – 2 Cr
- Femtosecond laser – 3 Cr
- Laser and mechanical dicing – 3 Cr
- CNC prototyping machine – 2 Cr

5-Year Plan with Milestones

Milestones	Year 1	Year 2	Year 3	Year 4	Year 5
Submit Proposal					
Identify industry partners					
Set up industry consortium					
Set up infrastructure					
Develop Research Programs					
Develop Educational Programs					
Demonstrate Technologies					
Integrate Technologies into Industry Prototype 1					
Integrate Technologies into Industry Prototype 2					
Integrate Technologies into Industry Prototype 3					

5-year budget for Co-Packaged Optics

Budget Categories	CPO SRA	Justification
1. Infrastructure Equipment Installation Building	80	Equipment and AMC – 75 Cr Building + Installation + lab infrastructure - 5 Cr
2. Research Projects	8.75	7 projects @ 25 lakhs pa/ project
3. Manpower Research Faculty Company Engineers Operations Manager Central Secretary Financial	3.5	2 research faculty @18 lakhs pa/person, operations manager ~ 9 lakhs/pa, admin and financial secretary ~8 lakhs pa, 4 technicians ; total ~ 70 lakhs pa
4. Students (Addl.)	7. 5	4 RA@75000 pm +10 JRF/PhD@48000 pm +30 MTech@15000 pm
5. Educ & Workforce	5	Hands-on training programs for students, workshops
6. Global Collaborators	2	2 Collaborators @100 lakhs/pa
7. Travel (Dom. & Intl.)	2.5	10 lakhs pa (national+ international) per project
8. Infra for Satellite Centers	15	Satellite center @ IIT Madras
Total (in INR Crores)	~124.5 Cr	

Optics Evolution

- (1) is clearly mainstream today
- (2) has experienced limited adoption
- High demands and rapid evolution of AI is driving to an immediate jump to (3) and (4) which minimizes the power of the electrical interface
- Already seeing adoption at the switch level
- Expectation is adoption at the compute level in the very near future