# IC & Board Assembly and Reliability

## Industry Co-Development Center (ICC) with Industry Consortium for Next Gen Research and Workforce


Nilesh Badwe, IIT Kanpur (Lead)

Shiv Govind Singh, IIT Hyderabad (Co-Lead)

&

Pradeep Vempaty, Micron (Industry Lead)

Ravi Bhatkal, MacDermid Alpha (Industry Co-Lead)

&

Vanessa Smet, Georgia Tech University

Shubhra Bansal, Purdue University

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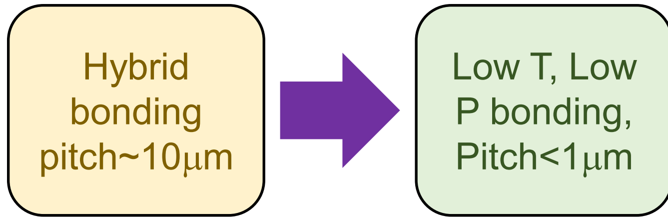
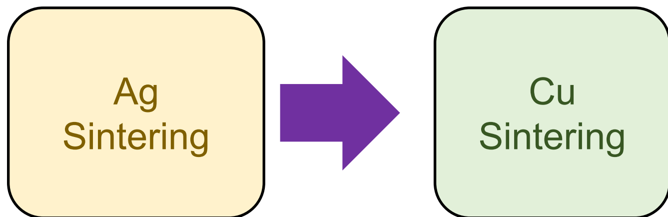
# Next Gen Industry Need and R&D Areas

## IC Assembly

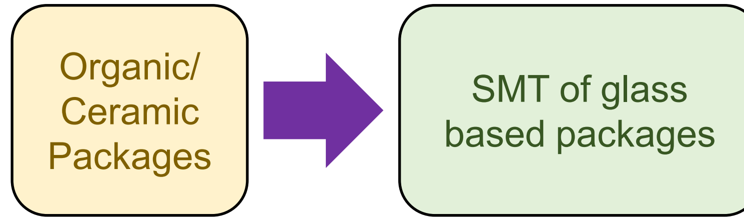



**Computing**

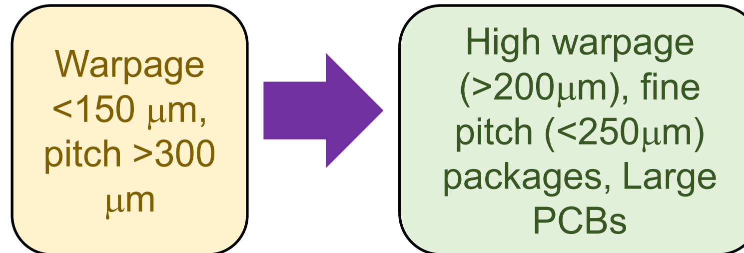



**Power Electronics**

## Board Assembly

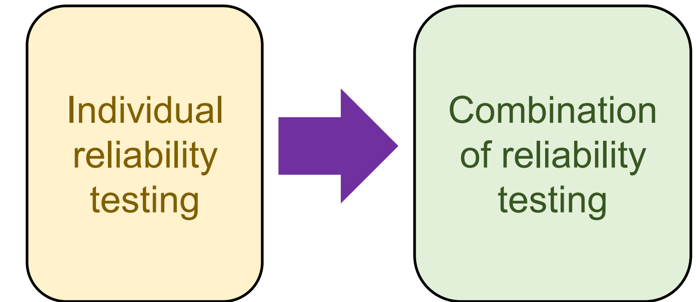



**Computing and 6G**




**Computing**

## Reliability




**Computing and Power Electronics**

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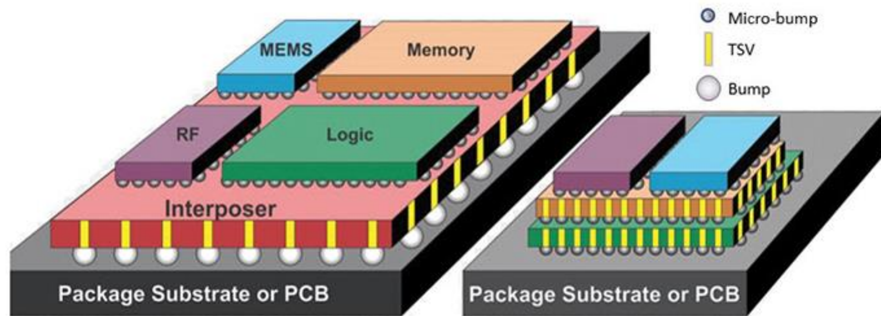
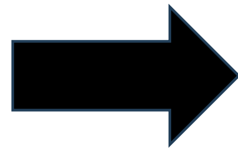
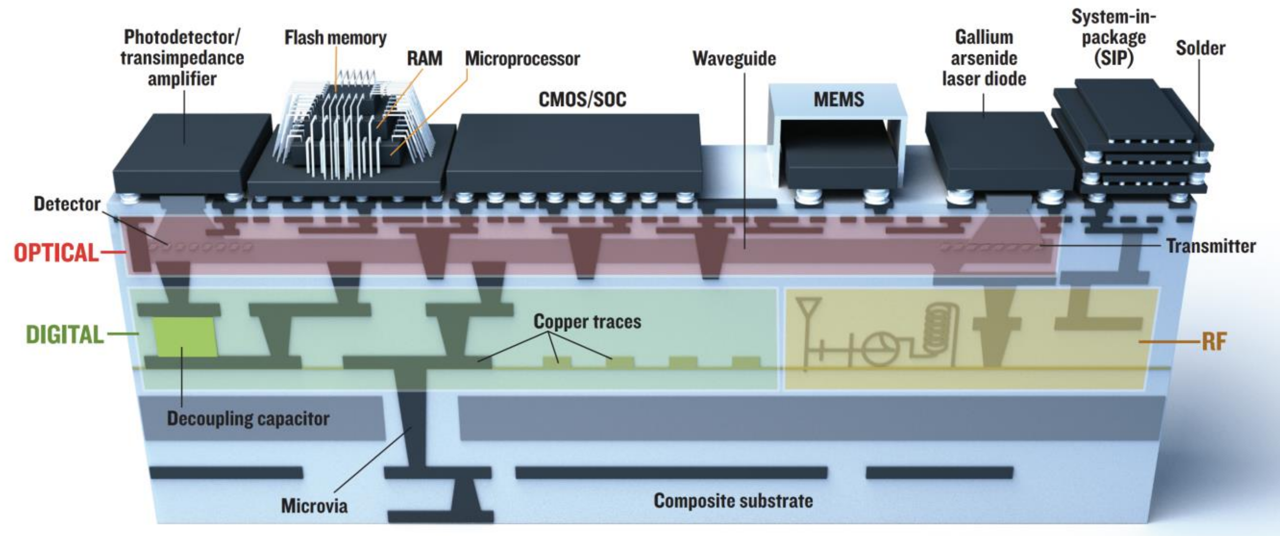
# Current State of the Art vs Proposed Futuristic Solution






2.5D and 3D Packaging

Multiple different types of modules on a single substrate within acceptable warpage limits meeting reliability requirements

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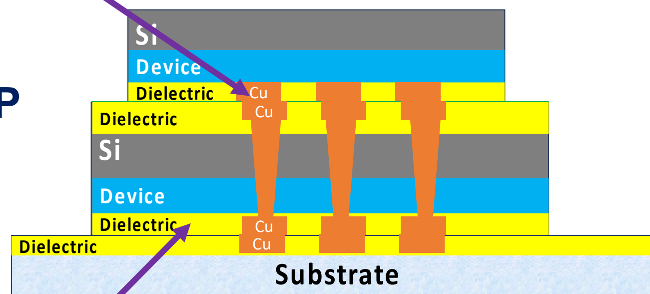
# Research Vision: Strategic Research Focus Areas

**Cu-Cu (Hybrid) bonding for IC Assembly**

Nilesh Badwe, IITK
Shiv Govind Singh, IITH
Poonam Sundriyal, IITKGP

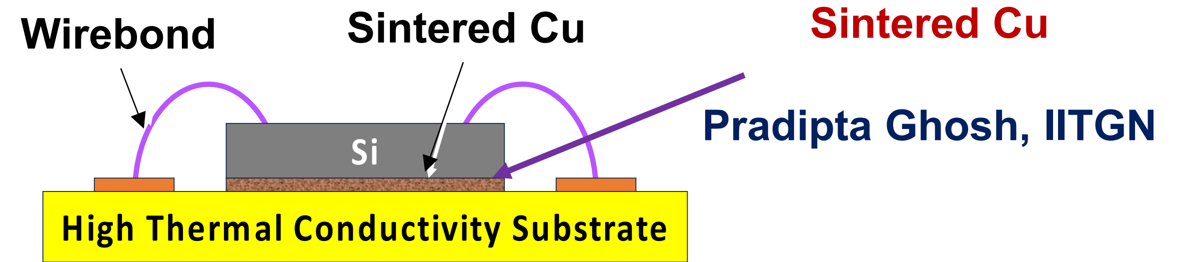
**Computing and AI**




**Dielectric materials (Underfills, Mold)**

Deepak Arora, IITJ

**Power Electronics**




Die Attach

**Sintered Cu**

Pradipta Ghosh, IITGN

**Electrical Reliability**

Shiv Govind Singh, IITH
Shanthi Prince, SRM

**Board Assembly**

Nilesh Badwe, IITK

**Thermomechanical Reliability**

Nilesh Badwe, IITK
Ajay Kumar, IITT
Pradipta Ghosh, IITGN

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# ICC Team: India-wide, multidisciplinary Faculty, Global Collaborators and Industry Partners

## Core Faculty Team

(Lead)

Nilesh Badwe
(MSE, IITK)

IC Assembly, Board Assembly, Thermo-mechanical reliability

(Co-lead)

Shiv Govind Singh
(EE, IITH)

IC Assembly, Electrical reliability

Pradipta Ghosh
(MSE, IITGN)

Sintered Cu

Poonam Sundriyal
(ME, IITKGP)

Surface modification for IC Assembly

Pradeep Dixit
(ME, IITB)

Low temp and TLP bonding

Deepak Arora
(CHE, IITJ)

Polymeric materials incl. underfill, molds

Shanthi Prince
(EE, SRM)

PCB design and reliability

Ajay Kumar
(ME, IITT)

Reliability of solders

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## Cross-SRA Faculty with releveant expertise

Pradeep Dixit
(ME, IITB)
Substrates

Bhagwati Prasad
(MSE, IISc)
Materials

Tarun Agarwal
(EE, IITGN)
Predictive modeling and design

# Hub and Spoke Model

IITJ: Underfill, Mold materials

IITK: Integration of digital packages (Computing) Thermomechanical rel

IITGN: Integration of power modules; Sintered Cu

IITKGP: Surface modification for IC Assembly

IITB: Low temperature bonding for IC assembly

IITH: Integration of optoelectronics packages; Electrical reliability

SRM: PCB Design and reliability

IITT: Materials Reliability

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इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF
ELECTRONICS AND
INFORMATION TECHNOLOGY

इंडिया सेमीकंडक्टर मिशन
India Semiconductor Mission
Catalyzing India's Semiconductor Ecosystem
Indian DSPS R&D Team. Together, We Can.

# Global Academic Collaborators

Prof. Vanessa Smet
Georgia Tech

- 3-D integration
- Interconnection and assembly processes
- SLID / TLP bonding
- All-Cu interconnections
- Low-temperature bonding
- Reliability

Prof. Shubhra Bansal
Purdue University

- Heterogeneous Integration & Advanced Packaging (sub-10 µm pitch interconnects, low-loss interposers)
- Harsh Environment Electronics Integration (high temperature Pb-free solders and nano-thermal interfaces)

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# COMPANY'S INTEREST IN RESEARCH & WORKFORCE IN THE ICBAR ICC

| | Company | Research Interest | Company Lead |
|---|---|---|---|
| IDMs and OEMs | Micron | Interconnects for FLI and SLI applications, reliability assessment | Pradeep V |
| | Intel | Cu-Cu bonding and board assembly for glass-based packages, low conductivity interconnects, low temp assembly, board assembly for complex shape packages and large PCBs, reliability | Arun C |
| | AMD | Cu-Cu bonding on glass substrates | Raja S |
| | Western Digital | Interconnects for FLI and SLI applications | Vinoth C |
| | Tata | Sintered Cu, Interconnect reliability | Kirubalan N |
| | Toyota | Sintered Cu, Combination of reliability testing | Shailesh J |
| | Infineon | Interconnects and reliability for power electronics | Vinay S |
| Material Suppliers | MacDermid Alpha | High reliability interconnects for low temperature applications, Sintered Cu, Board assembly and reliability | Ravi B |
| | Indium | | Andy M |
| | Baba Fine Chem | | Rakesh G |
| Equipment Suppliers | BESI | Cu-Cu bonding, Metrologies for improved processes and equipment accuracy | Jonathan A |
| | Lam Research | | Chee-Ping L |
| Design | Ansys | Material properties characterization for reliability modelling | Kajal K |

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# Educational Programs

## Current courses:

- Packaging courses @ IITK, IITB, IITKGP, IISc
- MTech Degree "Integrated Circuits and Microsystems Packaging" @ IITH
  - Introduction to IC Packaging
  - Fundamentals of IC Packaging Assembly and Manufacturing
  - IC Package Design for Manufacturing
  - Fracture and fatigue in electronic packaging
  - IC Fabrication Technology
  - Materials for Packaging
  - Electronic Package Design
  - Heat transfer in electronic packaging
  - IC Assembly and Characterization Lab
  - Experimental stress analysis Lab

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| Expected Workforce Development | | |
|---|---|---|
| Year | 5 Years | 10 Years |
| B Techs | 30 | 60-75 |
| M Techs | 30 | 60-75 |
| PhDs | 20 | 40-50 |

1 B.Tech., 1 M.Tech. and 1 Ph.D. student per project

**Duration:**

B.Tech. student: 1 Year
M.Tech. student: 2 Years
Ph.D. student: 5 Years

## Future Plan:

- Online MTech
- Post-Graduate level:
  - Masters and PhD students working on industry relevant challenges
  - A dedicated course focusing on the IC & Board Assembly and Reliability
  - New courses on Statistical Process control
  - Online courses/workshops
- Undergraduate level:
  - Elective courses
  - Hands-on training on IC assembly, Board Assembly and different reliability techniques through lab courses

# IIT Kanpur Packaging Course

| No. | Topics | Hours |
|---|---|---|
| 1 | Overview of IC Fabrication, Moore's law, Introduction to Semiconductor Packaging, Packaging eras, Moore's law for packaging, 2.5D and 3D packaging technologies, Types of packages (DIP, QFN, QFP, LCC, LGA, PGA, BGA) | 5 |
| 2 | Design aspects of packaging: Electrical design for signal and power integrity, Materials and manufacturing of passive components, Heat transfer in packaging/Thermal design, Fundamentals of test | 6 |
| 3 | Substrate architecture, Basics of ceramics, organic, glass, and silicon-based package substrates | 4 |
| 4 | Die-prep processing: backgrinding and dicing, Chip-to-package interconnections and assembly, Encapsulation: Underfill and mold materials | 6 |
| 5 | Fundamentals of board assembly: Types of PCBs, PCB design, Materials and processes in board assembly, SMT defects and mitigation paths, Fluxes, Solder alloys (Sn-Pb, SAC, SnBi, high reliability), Solder pastes | 4 |
| 6 | Reliability testing: Thermomechanical, Mechanical shock, Electromigration, Characterization/failure analysis techniques in packaging (microscopy, surface characterization, physical properties measurements techniques) | 4 |
| 7 | Basics of process engineering, Statistical process control | 3 |
| 8 | Advanced packaging techniques: Hybrid bonding, Heterogeneous Integration, Optical interconnects, Overview of latest research papers | 3 |
| 9 | Specialized applications: Computing, Quantum technology, Memory, Power electronics/Automotive, Flexible electronics, MEMS & Sensors | 5 |
| 10 | Project: Cross-section and Failure analysis of different packages | 2 |

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- Covers basics of Semiconductor Packaging with a special focus on materials and manufacturing
- Continuous improvement in the curriculum based on industry inputs
  - Process engineering, statistical process control
- Expert lectures from external industry and academia
  - Pooya Tadayon (Intel), Nachiket Raravikar (Mojo vision), Anandaroop Bhattacharya (IITKGP), Rohit Sharma (IITRPR)
- Exposure for students to industry relevant problems
  - Collaboration with Ansys, Micron, and Intel for course project

# Proposed R&D Areas - 1

## 1. Design (Electrical, Mechanical) at Assembly Level

- AI assisted modeling and design of optimized package for system level reliability and warpage management

## 2. Advanced Materials and Processes

- Low/ultra-low temperature board level assembly materials and processes
- High throughput Cu-Cu bonding at fine pitch incl. hybrid sintered bonding for large panels, glass to wafer bonding, etc.
- Board assembly and reliability of packages with complex warpage profiles (thin dies, 3D ICs, etc), large size boards
- Application specific material development (interconnects, molding/adhesives, die attach films) for warpage management at different temperatures
- Interconnect material development for quantum computing (ultra-low temperature applications)
- Sintered Cu (mixed size powder, nanoporous Cu, electric field assisted sintering)
- High reliability interconnect materials and technologies for both first level and second level interconnects
- Low temp, low pressure Cu-Cu bonding for PCB level

## 3. Advanced Prototyping

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- Design and demonstrate prototypes for advanced materials and processes

# Proposed R&D Areas - 2

## 4. Metrology and Characterization

- General material property characterization incl thermal, electrical conductivity, mechanical properties
- Adhesion characterization for different interfaces in a package: die bonding/attach
- Identification of critical failures in a package
- Metrology for placement accuracy of stacked dies
- Process simulation (UF flow, flux clean, etc.)

## 5. Reliability

- Stacked dies: dynamic warpage, Rel with LTS, electromigration with LTS linking to AI assisted modeling
- DBC substrates for power electronics, its impact of TC
- Electromigration in sintered Ag, Cu, generally power electronics
- Thermal cycling (ultra low temp, ultra high temp), ageing, shock, vibration, power cycling/electromigration, combination of rel testing
- Failure mechanism understanding

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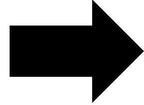
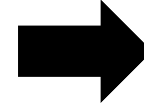
# Process Flow for IC Assembly

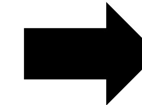
**Patterning on wafer for bonding**



**Advanced backgrinding and dicing**



**Assembly: Flip chip incl hybrid bonding, Wire bonding**



**Failure analysis/ Characterization**

| Patterning on wafer for bonding | Advanced backgrinding and dicing | Assembly: Flip chip incl hybrid bonding, Wire bonding | Failure analysis/ Characterization |
|---|---|---|---|
| Spin coater | Tape lamination w/ UV cure | Die pick and place | X-section, polishing |
| Mask maker | Advanced back-grinding/ polishing tool | Flip chip bonder | Optical and confocal microscopes |
| Aligner | Advanced dicing machine (Plasma, stealth, laser, ultrasonic) | Wafer bonder | Shadow Moire |
| Electrodeposition | DI water system | Wirebond | CSAM |
| Sputtering | CMP | Molding | SEM-FIB w/ EBSD & EDS |
| Evaporator | | Underfill dispense | X ray fluorescence |
| Plasma | | Curing ovens with environment control | TOFSIMS |
| Wet bench | | | I-V Prober |
| | | | UTM, Shear tester |

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# Process Flow for Board Assembly

**Creating complex shape/warpage BGA packages** → **Large/Thin Printed Circuit Boards (PCBs)** → **SMT Process Development/ Hammer Tests** → **Failure analysis/ Characterization**

| Creating complex shape/warpage BGA packages | Large/Thin Printed Circuit Boards (PCBs) | SMT Process Development/ Hammer Tests | Failure analysis/ Characterization |
|---|---|---|---|
| IC Assembly process tools<br>BGA sphere attach<br>Package design and simulation tools | PCB design software<br>PCBs will be sourced commercially | ***Existing facilities***<br>Loaders and unloaders<br>Conveyors<br>Solder paste printer<br>Solder paste inspection<br>Pick and place<br>Reflow oven<br>Automated optical inspection tool | IC assembly related tools<br>Dye and Pry<br>3D X-Ray inspection |



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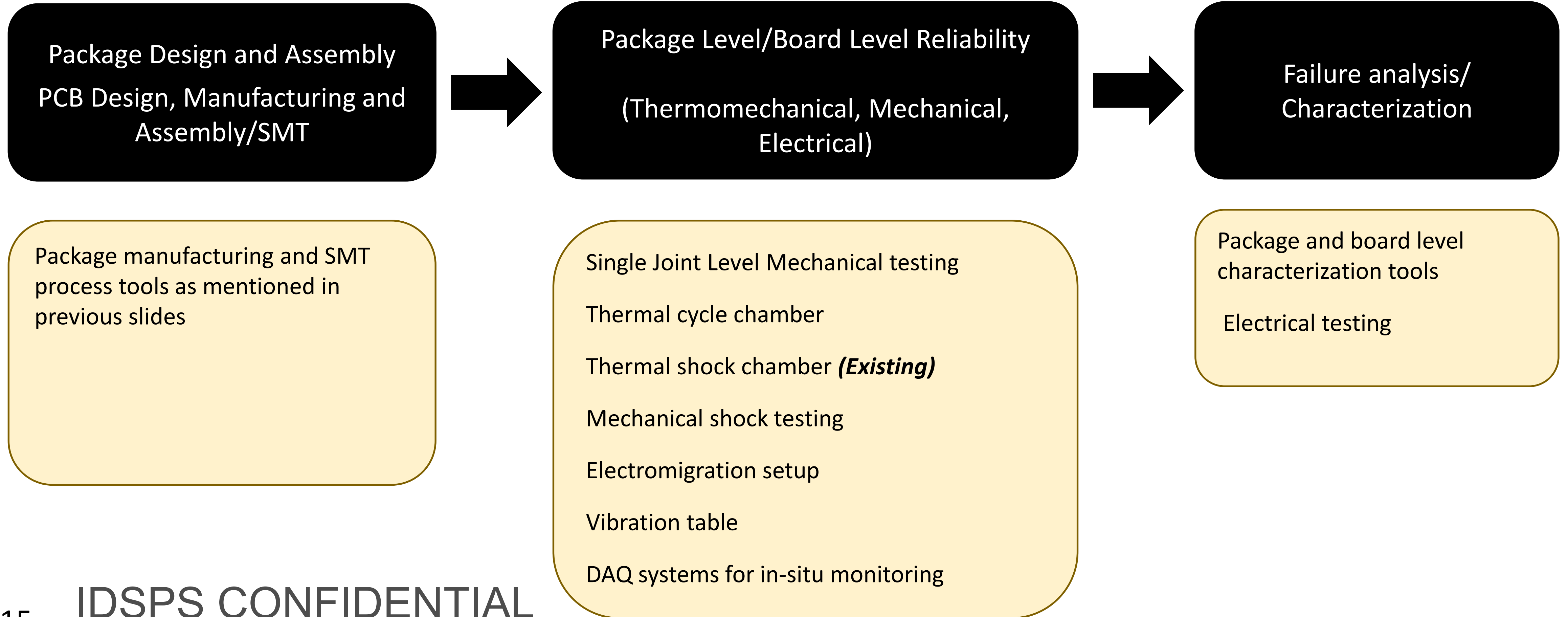
# Process Flow for Reliability

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# MacDermid Alpha Thermal Reliability Laboratory

- Initiated through the Corporate Social Responsibility (CSR) initiative of MacDermid Alpha
- Focus on skills development and research support for “Thermomechanical reliability assessment of electronic components”
- Capabilities:
    - Thermal shock testing with in-situ monitoring,
    - Aging/baking oven
    - Failure analysis facilities including PCB cross-sectioning/Diamond saw cutter, sample mounting, dual motor polishing wheel
    - Advanced Digital Microscope

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# NMTronics Center of Excellence for Electronics Manufacturing and Skills Development

- Initiated through the Corporate Social Responsibility (CSR) initiative of NMTronics India Pvt. Ltd.
- Focus on skills development, manufacturing support and research related to Electronics Manufacturing, specifically Surface Mount Technology (SMT)
- Capabilities: State-of-the-art Surface Mount Technology line including solder paste printing, solder paste inspection, pick-and-place, reflow oven, automated optical inspection
- Certificate courses at different levels including technician/operators, process engineers, and administrators/management
- Manufacturing and R&D support to industries including start-ups

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# Semiconductor Packaging Laboratory

- Planned
- Primary focus on skills development for Semiconductor Packaging
- Planned Facilities:
  - Clean room
  - Design simulation packages,
  - Wafer processing: Polishing, Dicing, Pick and place
  - IC assembly: Wirebonder, Die bonder, Molding
  - System assembly
  - Reliability and failure analysis: Thermal cycle, mechanical shock, vibration tables, cross-sectioning, optical and electron microscopes

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# List of Projects

1. Design and Demonstrate Low Temperature Fine Pitch Cu-Cu
2. Bonding on Si/Glass to Glass
3. Design and Demonstrate Low Temperature Low Pressure Nb-Nb bonding for Large Scale Qubits Integration
4. Adhesion improvement of Cu-Cu and Cu-Epoxy joints
5. Development of Low Temperature Indium-based wafer-level Bonding
6. Process Development of Sintered Cu and alloys for Die attachment application in Power Electronics
7. Systematic study of temperature-dependent properties of Sn-Bi-based low-temperature solder alloys with various alloying elements
8. Study on Optimization of High Temperature Solder Alloys Composition and Reliability Evaluation in Power Semiconductors
9. Combined Effect of Fatigue and Current on the Reliability of a SnBi based Low Temperature Solder Joints
10. Low Temperature Cu-Cu Bonding at PCB Level
11. Reliability Analysis of a Printed Circuit Board (PCB), Electronic Components and ICs

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# Design and Demonstrate Low Temperature Fine Pitch Cu-Cu Bonding on Si/Glass to Glass

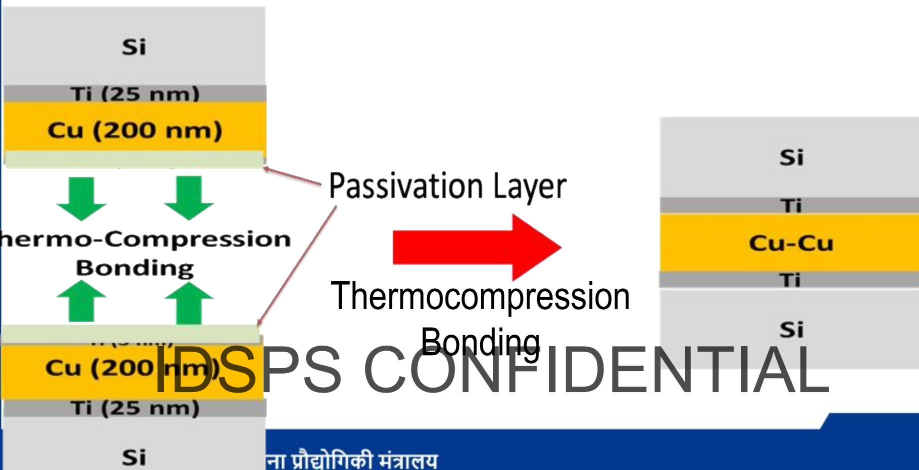
**PIs: Shiv Govind Singh (IITH), Nilesh Badwe (IITK), Vanessa Smet (GaTech)**

## Objective

- To develop and demonstrate ultra fine pitch VIA formation and filling in thin glass substrate.
- Surface engineering for low temperature low pressure bonding Cu-Cu Si/Glass -Glass Thermocompression Bonding.
- Electrical, Mechanical and reliabilities studies of interconnects.

| Parameters | Current state of the art (Cu-to Cu Wafer to wafer bonding) | Proposed (Cu- Cu, Si/Glass - Glass bonding) |
| --- | --- | --- |
| **TGV diameter formation** | 15um | 10-15um |
| **Bonding temperature** | <200 °C | <250 °C |
| **Bonding pressure** | <10 M Pascal | <10 M Pascal |
| **Pitch** | < 25micron | < 25micron |
| **Specific Contact Resistance** | < 10-7 ohm/cm$^2$ | < 10-7 ohm/cm$^2$ |

**WP1:** Surface engineering for low temperature low pressure Cu-Cu Bonding at Si/Glass- Glass bonding

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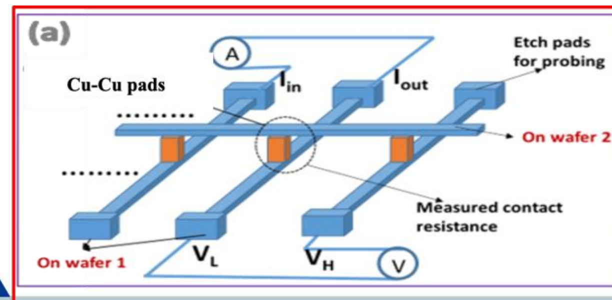
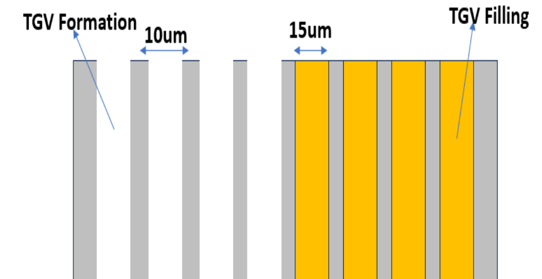
## Approach

**WP2:** Electrical, Mechanical and reliabilities studies of interconnects




**WP3:** Ultra fine pitch VIA formation and filling in thin glass substrate.




Panigrahy, A.K., Ghosh, T., Vanjari, S.R.K. and Singh, S.G., 2019. *IEEE Transactions on Device and Materials Reliability*, *19*(4), pp.791-795.
Cheemalamarri, H.K., Sundaram, A., Anh, T.V.N., Ok, Y.J., Rao, V.S. and Singh, N., 2024, May.. In *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)* (pp. 1543-1547). IEEE.

# Design and Demonstrate Low Temperature Low Pressure Nb-Nb bonding for Large Scale Qubits Integration

PI: Shiv Govind Singh (IITH), Naresh Emani (IITH), Nilesh Badwe (IITK), Vanessa Smet (GaTech)

## Objective

- Selection of optimized superconducting interconnect materials using simulation.
- Demonstration of Low-temperature Low-pressure thermocompression bonding of selected materials.
- Electrical, Mechanical, and Reliability Studies of superconducting interconnects.

## Proposed vs. Prior Art

| Parameters | Current Status | Proposed |
|---|---|---|
| Interconnect materials | Cu (however not suitable as Cu is not SC materials), Nb as well | Nb and still doing more simulation |
| Bonding temperature | Cu 150, Nb room temperature SAB treatment, | <250$^0$C, |
| Bonding pressure | Cu , 9 MPascal, Nb npt reported | Sub 10 MPascal |
| Bond strength | Cu 113Mpascal , Not reported | >100M Pascal |
| Pitch | Cu, 25 um, Nb Not reported | <50 micron |
| Specific Contact Resistance | <10$^{-7}$ohm/cm$^2$ Cu, Nb, Not reported | < 10$^{-5}$ ohm/cm2, SC below $T_C$ |

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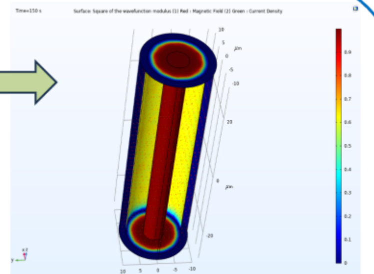
## PROPOSED APPROACH CONTINUED

### Objective -1

**Selection of optimized Superconducting Material**

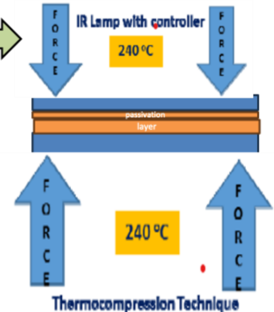


Problem:- Interlayer dielectrics (ILDs) to isolate signals from multilayers like silicon dioxide, and silicon nitride decrease qubit lifetimes

Solution:- Material compatible with high-coherence qubits (Modelling and Simulation of **Nb/ other superconducting material**).

### Objective-2

**Integrate the qubit Chip and interposer**

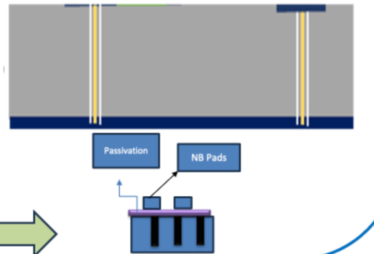



Problem:- Copper is not superconducting hence metallization and electric current in these metals cause heating and exciting Quasiparticle results in qubit performance degradation

Solution:- Bonding of less lossy superconducting material like Nb/ other superconducting Material (Direct Bonding or using a Passivation Layer)

### Objective- 3

**Electrical, Mechanical, and Reliability of Superconducting Bonding Interface and Array of SC Interconnect**



Problem:- Electrical, Mechanical, and reliability study at Cryogenic Temperature.

Solution:- AFM, XRD, C-SAM, SEM, EDX, and Cryogenic Test for material characterization, shear/pull test for Mechanical Characterization, I-V (normal and SC ), electromigration test, qubit coherence analysis using microwave generator.

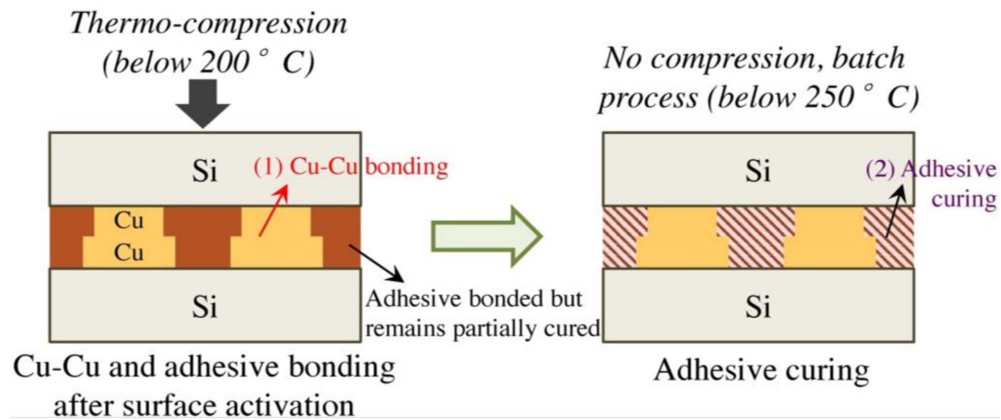
Fujino, M., Araga, Y., Nakagawa, H., Takahashi, Y., Nanba, K., Yamaguchi, A., Miyata, A., Nishi, T. and Kikuchi, K., 2023. interconnects. Journal of Applied Physics, 133(1).

Renaud, P., Dubarry, C., Bresson, N., Deschaseaux, E., Fournel, F., Morales, C., Abadie, K., Thomas, C. and Charbonnier, J., 2024, May. In *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)* (pp. 441-446). IEEE.

# Adhesion improvement of Cu-Cu and Cu-Epoxy joints

PI: Poonam Sundriyal (IITKGP), Deepak Arora (IITJ), Nilesh Badwe (IITK)

**Objective:** Surface activation of Cu to improve to improve the adhesion between Cu-Cu and Cu-Epoxy joints at low temperature (room temperature to 150°C).




*Adapted from Suga et al., 2021.*

## Proposed vs. Prior Art

| Parameters | Current state of the art | Proposed |
|---|---|---|
| **Shear strength** | 56 MPa | >100 MPa |
| **Temperature range** | >450 °C | Room temperature to 200 °C |
| **Wettability and Surface energy** | ~ 60 to 85° and low surface energy | ~ 10° and high surface energy |

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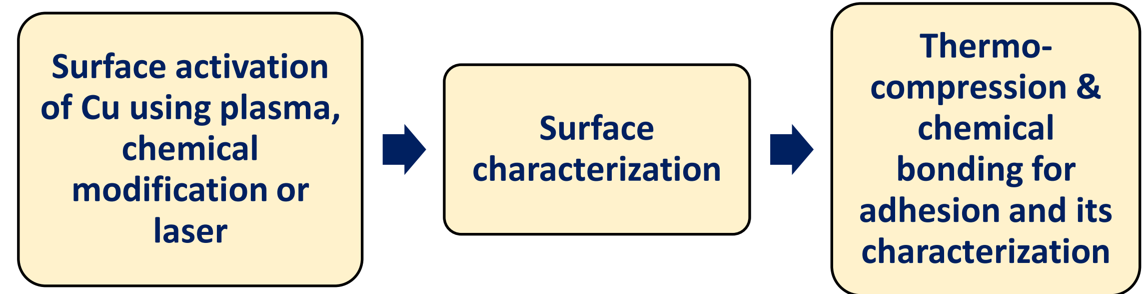
## Approach

- The surface activation of Cu using chemical treatment, plasma, passivation, and Laser texturing.
- The surface roughness, surface energy, and functional groups of surface will be manipulated.
- The activated surfaces will form strong chemical joints at room temperature




## Outcome and Impact

- Demonstration of a suitable surface activation techniques of copper for adhesion improvement.
- Better interface adhesion will improve the quality and reliability of 3D interconnects.

Kim, S., Nam, Y. and Kim, S.E., 2016. Japanese Journal of Applied Physics, 55(6S3), p.06JC02.
Chua, S.L., Chan, J.M., Goh, S.C.K. and Tan, C.S., 2018. IEEE Transactions on Components, Packaging and Manufacturing Technology, 9(3), pp.596-605.

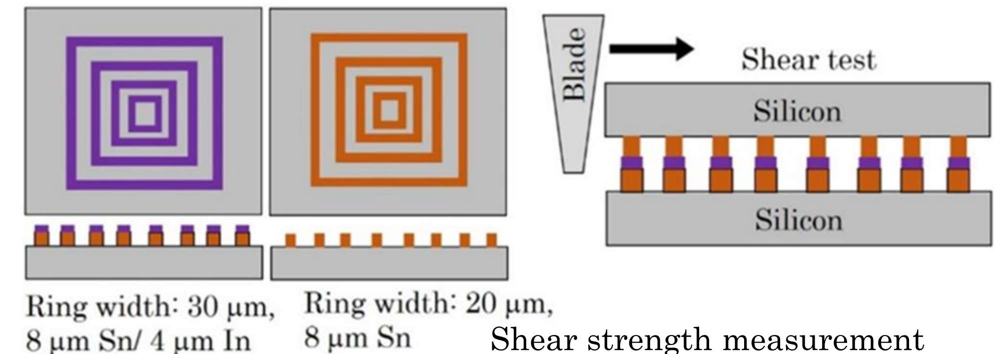
# Development of Low Temperature Indium-based wafer-level Bonding

PI: Pradeep Dixit (IIT Bombay)

Objective: To develop and demonstrate low-temperature (<200°C) Indium-based bonding for wafer-level packaging

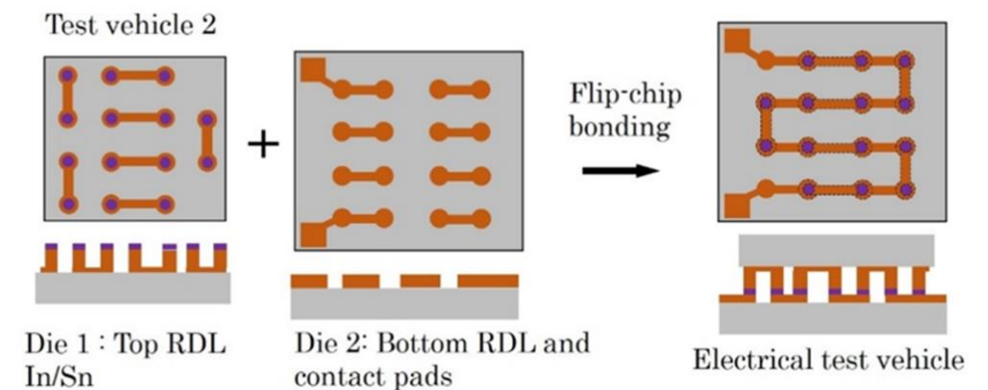
Prior art Vs proposed R&D:

| | Current state | Proposed |
|---|---|---|
| Material | Sn-based solder alloys | In-based alloys |
| Pitch | < 50 μm | < 50 μm |
| Bonding temperature | >250 °C | <200 °C |
| Uniformity | ±5 % | ±5 % |




Technical Challenges:

- ❑ Demonstrate wafer-scale indium electroplating with ±5 % uniformity
- ❑ Solder based flip chip bonding for fine pitch and low temperature bonding
- ❑ Wet chemical etching of seed layer without affecting indium bumps
- ❑ Reliability of low temp bonded-assembly

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# Process Development of Sintered Cu and alloys for Die attachment application in Power Electronics

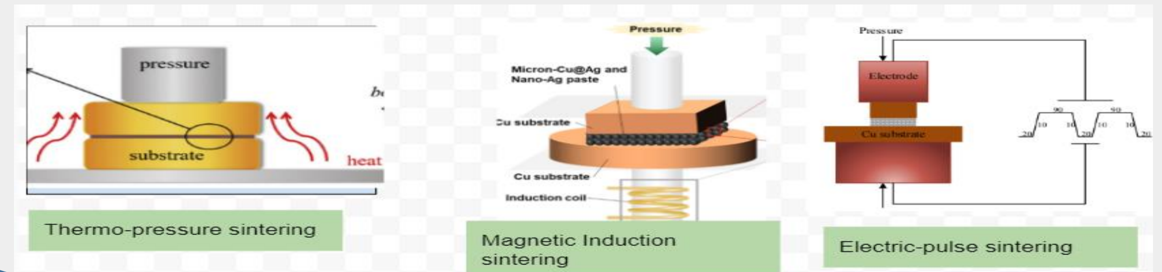
Pradipta Ghosh (IITGN), Komal Kumar (IITGN), Nilesh Badwe (IITK)

**Objective:** Discover new alloys and develop processes for defect free die attachment for high temperature (>300°C) Power electronics.

- Identify proper material and sintering environment for low sintering temperature (150°C-250°C)
- Explore different heating methods for sintering and quantify their effect on kinetics of sintering
- Quantify the thermo-mechanical reliability and electromigration in sintered material

**Proposed Method:** Thermo pressure based sintering of Cu powders, Cu@Ag powder with reducing agents using:

(1) Thermo-pressure sintering
(2) Electric pulse sintering
(3) Magnetic induction sintering




## Industry need:

| Material and Process | Advantages | Disadvantages |
|---|---|---|
| High Temperature Solders (Au-In, Ag-Au-Ge, Ag-Cu eutectics) | High $T_{Operation}$ | High $T_{bonding}$, Cost |
| TLP Bonding (Ag/In, Au-In) | Low $T_{Bonding}$ and high $T_{Operation}$ | Long Bonding time, Void formtion, Brittle IMC |
| Ag/Cu powder sintering | Low $T_{Bonding}$ and high $T_{Operation}$ | Ag (Costly, electromigration); Cu (oxidation) |

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## Comparison of Proposed and Prior art:

| Parameters | Current state of the art | Proposed |
|---|---|---|
| Conventional Sintering T (°C)/ time (min)/ P (MPa) | 300-500/ 5-15/ ~10-40 | < 250/ ~1-5/<5 |
| Electric pulse assisted sintering CD ($A.mm^{-2}$) | 200 for copper powders | Thermal + current Cu-NP size, chemistry |
| Induction heating | Ag powders<br>Ag coated Cu powders | Cu-NP, Cu@Ag<br>size, chemistry |

# Systematic study of temperature-dependent properties of Sn-Bi-based low-temperature solder alloys with various alloying elements

Nilesh Badwe (IITK), Pradipta Ghosh (IITGN), Shiv Govind Singh (IITH)

## Objective

To create a knowledge base of the impact of different alloying elements and their concentrations on the physical and mechanical properties of SnBi based low temperature solders (LTS) over a temperature range relevant to electronics

## Approach

- **Synthesis** of the Sn-Bi-based LTS Solder doped with Ag, Cu, Sb, In, Co, and Ni with concentrations 0-1 wt.% respectively
- **Microstructural Characterization:** IMC thickness/composition on CuOSP and ENIG substrate coupon pre and post ageing
- **Physical properties:** Resistivity, Temperature coefficient of resistance, Melting and solidification behaviour
- **Thermomechanical Properties:** Tensile testing and low cycle fatigue testing at (-40°C, -20°C, 0°C, 25°C, 85°C, 100°C)

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## Proposed vs Prior Art

| Parameters | Composition | Current state of Art | Proposed |
|---|---|---|---|
| Temperature-dependent tensile properties | Eutectic Sn-58Bi | Limited | Yes |
| | Other alloying elements | No | Yes |
| Temperature-dependent fatigue performance | Eutectic Sn-58Bi | No | Yes |
| | Other alloying elements | No | Yes |
| Temperature dependant resistivity | Eutectic Sn-58Bi | Limited | Yes |
| | Other alloying elements | No | Yes |

Kamaruzzaman, L.S. and Goh, Y., 2022. *Soldering & Surface Mount Technology*, *34*(5), pp.300-318.
Mokhtari, O. and Nishikawa, H., 2016. *Materials Science and Engineering: A*, *651*, pp.831-839.

# Study on Optimization of High Temperature Solder Alloys Composition and Reliability Evaluation in Power Semiconductors

Ajay Kumar (IITT), Nilesh Badwe (IITK)

- **Objective:** To optimize the composition of high-temperature solder alloys and study their long-term reliability

## Approach:

- **Synthesis:** Select appropriate solder alloy compositions and design based on the impact of extreme conditions on the reliability and durability of solder joints
- **Characterization and Testing:**
- Microstructure evolution, Interfacial reactions, characteristics of IMCs
- Mechanical shear performance, creep resistance and failure analysis
- Corrosion resistance
- The creep strength at the reliability design stage of the packaging (300$^{o}$C-400$^{o}$C)
- Reliability mapping

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## Proposed Vs Prior Art:

| Parameters | Composition | Current State of Art | Proposed |
|---|---|---|---|
| Long-term reliability at high-temperature | Au–Sn, Au–Ge, Zn–Al, Zn–Sn, Sn–Sb, Bi–Ag | No | Yes |
| Creep Resistance | Au–Sn | No | Yes |
| Interfacial reactions, characteristics of IMCs | Au–Ge, Au-In, Ag-Cu | No | Yes |
| Grain size control, corrosion resistance | Zn–Al, Zn–Sn | No | Yes |
| Interfacial reaction and solder joint strength | Sn–Sb, Au-Ag-Ge, Bi-Ag | No | Yes |

Reliability and Durability

Extended Operational Lifespan

Manufacturability and Cost Savings

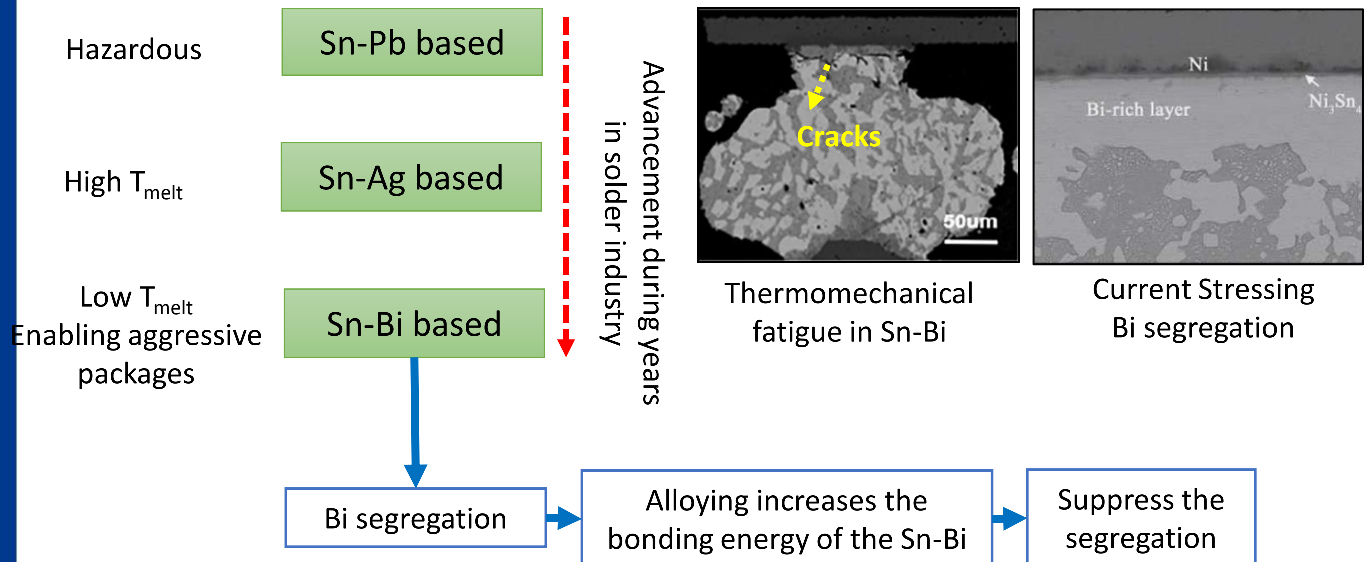
Reduced Downtime

1.Morshed, M, Y Wang, L R. Billa, T Grant, M Mat, and D Payne" In *PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 1-5. VDE, 2023.
2.Zeng, G, S McDonald, and K Nogita." *Microelectronics Reliability* 52, no. 7 (2012): 1306-1322.

# Combined Effect of Fatigue and Current on the Reliability of a SnBi based Low Temperature Solder Joints

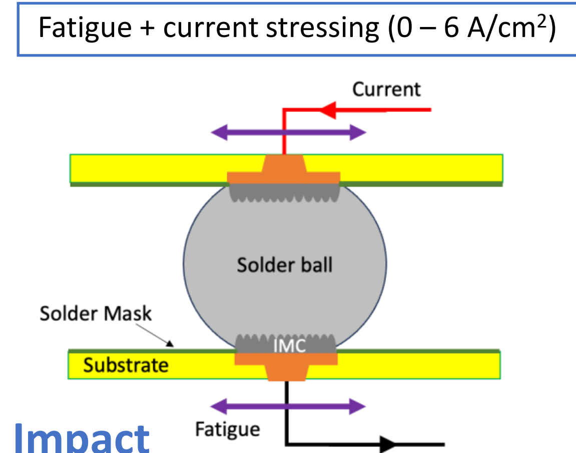
**Nilesh Badwe (IITK), Ajay Kumar (IITT) and Pradipta Ghosh (IITGN)**

**Objective -** To study the combined effect of fatigue and current on the life of Sn-Bi based solder alloy joint with a focus on performance improvement through alloying elements Sb, In, and Ag




## Approach

- Alloying of 0-1% of Sb, In & Ag homogenization through multiple melting cycle
- Solder joint formation through preforms




## Proposed vs. Prior Art

| Parameters | Current State | Proposed |
|---|---|---|
| Combined effect of fatigue and current | Package level | Controlled joint level |
| Effect of alloying elements on fatigue and current stressing | No | Yes |
| Solder joint level study to include IMC impact | No | Yes |

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## Outcome and Impact

- Study the effect of failure mechanism and effect of alloying
- Design, synthesis, and characterization
- Model development to separate the effect of current and fatigue on an individual solder joint life

Surendar, A., Kishore, K.H., Kavitha, M., Ibatova, A.Z. and Samavatian, V., 2018.. *IEEE Transactions on Device and Materials Reliability*, *18*(4), pp.606-612
Long, X., Liu, Y., Jia, F., Wu, Y., Fu, Y. and Zhou, C., 2019. *Journal of Materials Science: Materials in Electronics*, *30*, pp.7654-7664..

# Low Temperature Cu-Cu Bonding at PCB Level

PIs: Shiv Govind Singh (IITH), Nilesh Badwe (IITK), Vanessa Smet (GaTech)

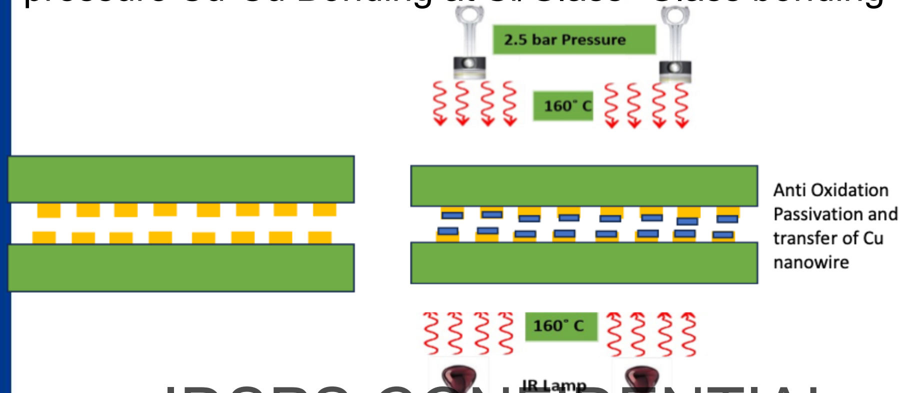
**Objective**

- Design and fabricate Cu pad at PCB akin to normal PCB used for assembly.
- Surface engineering for demonstration of low temperature low pressure bonding.
- Electrical, Mechanical and reliabilities studies of interconnects.

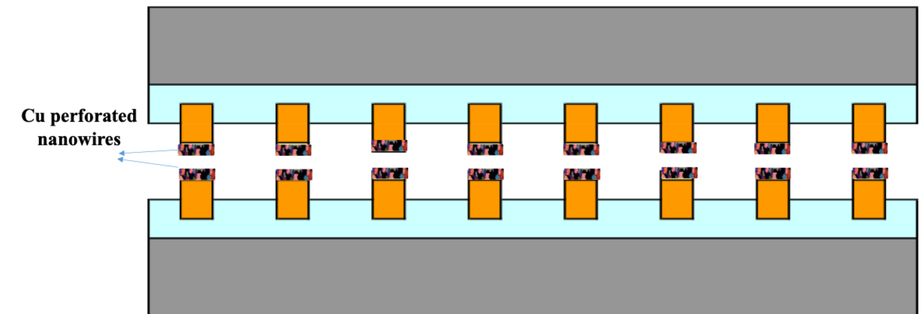
| Parameters | Current state of the art (Solder bonding/ paste) | Proposed (solderless bonding) |
|---|---|---|
| Cu-Cu bonding PCB level | Solder use, ~160$^{O}$ | < 200$^{0}$C |
| Bond strength | 8 - 18 MPa | > 50 MPa |
| Bonding Pressure | 0 - 1.8 MPa | < 2 MPa |
| Pitch | 100 $\mu$m | < 50 $\mu$m |
| Cu Trace | ~ 50 $\mu$m/Blanket | 25 $\mu$m |

**WP1:** Surface engineering for low temperature low pressure Cu-Cu Bonding at Si/Glass- Glass bonding

**Approach**




**WP2:** Warpage utilize perforated Cu nanowires on top of Cu pad/ trace to address the variation on top of surface passivation

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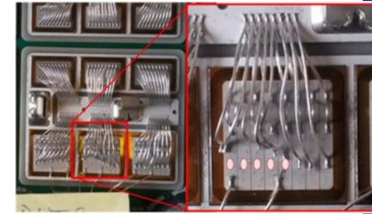
Cao, Z., Lehmann, J., Heusdens, B., Durmaz, E.C., Krüger, P., Wietstruck, M., Herfurth, N., Adesunkanmi, A.A., Carta, C. and Kaynak, M., 2024IEEE Transactions on Components, Packaging and Manufacturing Technology.

Jangam, S., Bajwa, A.A., Mogera, U., Ambhore, P., Colosimo, T., Chylak, B. and Iyer, S., 2019t. In *2019 IEEE 69th electronic components and technology conference (ECTC)* (pp. 620-627). IEEE.

# Reliability Analysis of a Printed Circuit Board (PCB), Electronic Components and ICs

Team: Dr. Soumyaranjan Routray (SRM), Prof. Shanthi Prince (SRM), Prof. P. Eswaran (SRM)



## Objectives:

- Reliability Analysis of Electronic Components and PCB using CAD Tool/DFT Anlysis
- Understanding the failure modes and failure mechanisms of PCB/Component failure
- Corrective Action to improve reliability

| | Current state* | Proposed |
|---|---|---|
| **Reliability Issue** | conductive anodic filament (CAF) | CAF Resistant |
| **Microcrack** | De-penalization | modified de-penalization method |
| **Electromagnetic Induced Failure** | Crack or Pit shape defects | Radiation resistant design for components |
| **Thermal Stress/Surface degradation** | Breakdown of components and Traps | Finding root cause of failure |

I. Hill, P. Chanawala, R. Singh, S. A. Sheikholeslam and A. Ivanov, "CMOS Reliability From Past to Future: A Survey of Requirements, Trends, and Prediction Methods," in *IEEE Transactions on Device and Materials Reliability*, vol. 22, no. 1, pp. 1-18, March 2022

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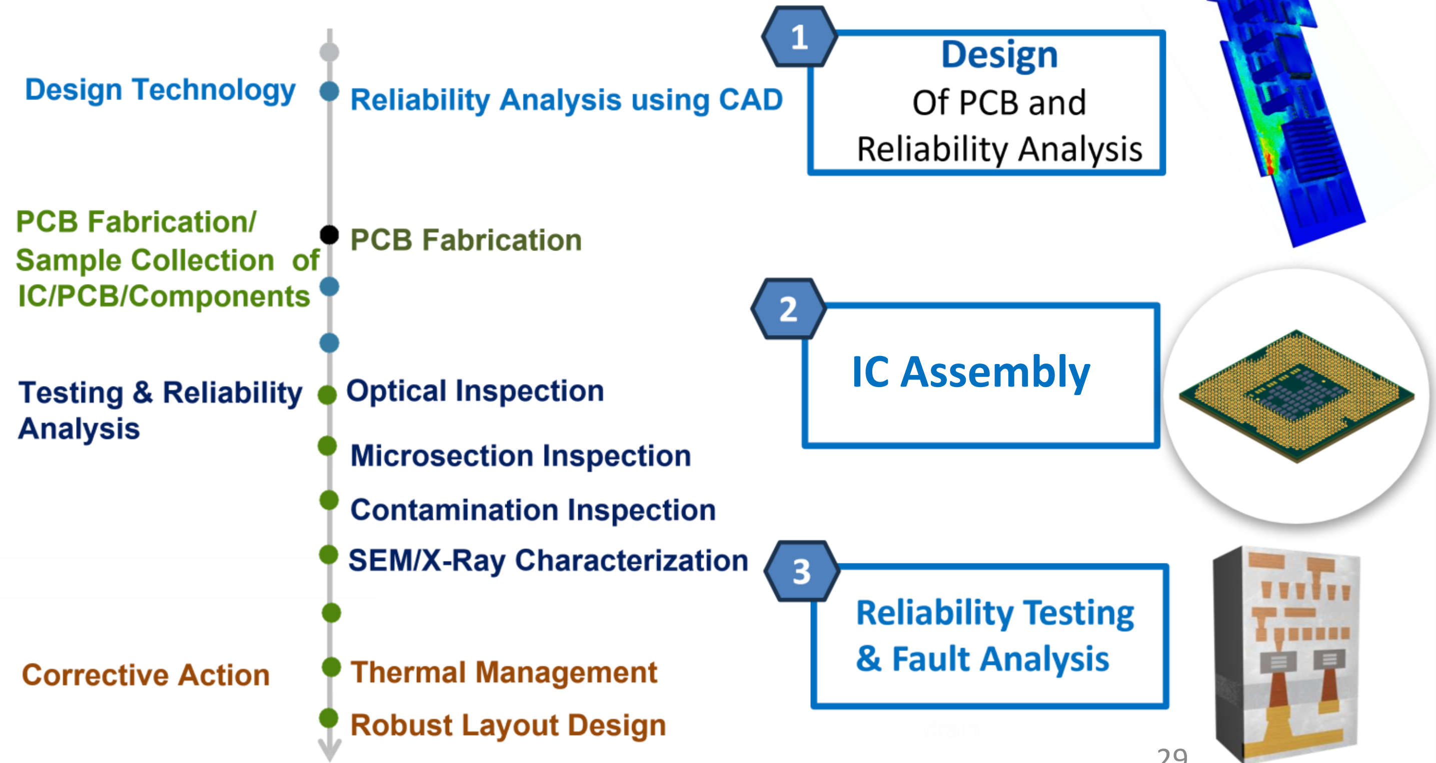
## Approach:




**Global Collaboration:**

**Prof. Cher Ming Tan**, Director, Centre for Reliability Sciences and Technologies (CreST), Chang Gung University, Taiwan

# 5 Year Plan/Timeline

| Milestones | Year 1 | Year 2 | Year 3 | Year 4 | Year 5 |
|---|---|---|---|---|---|
| Submit Proposal | | | | | |
| Identify industry partners | | | | | |
| Set up industry consortium | | | | | |
| Set up infrastructure | | | | | |
| Develop Research Programs | | | | | |
| Develop Educational Programs | | | | | |
| Demonstrate Technologies | | | | | |
| Integrate Technologies into Industry Prototype 1 | | | | | |
| Integrate Technologies into Industry Prototype 2 | | | | | |
| Integrate Technologies into Industry Prototype 3 | | | | | |

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# Industry Needs (Intel)

- SoC (Silicon area) for computing/AI is growing at an unprecedented rate → 2.5D, 3D & 3.5D
- Package area grows because of SoC (2.5x-4x) as well as I/O count and higher power (TDP) requirements
- >10K mm substrate area with 1000s of I/Os
- Higher I/O speed → GND pins → overall pin count and substrate size
- Assembly of large BGA → LTS → current carrying capability improvement

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