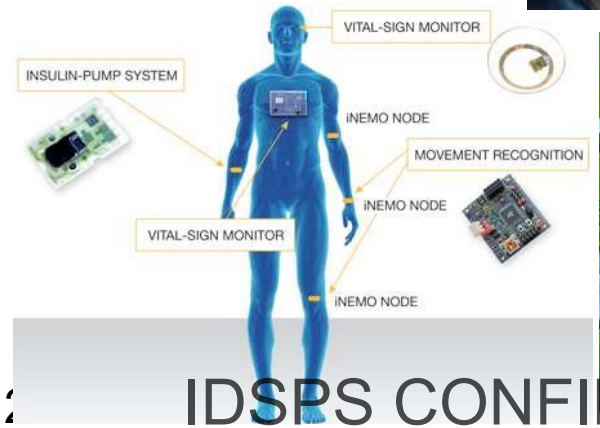
Next Generation CMOS Devices

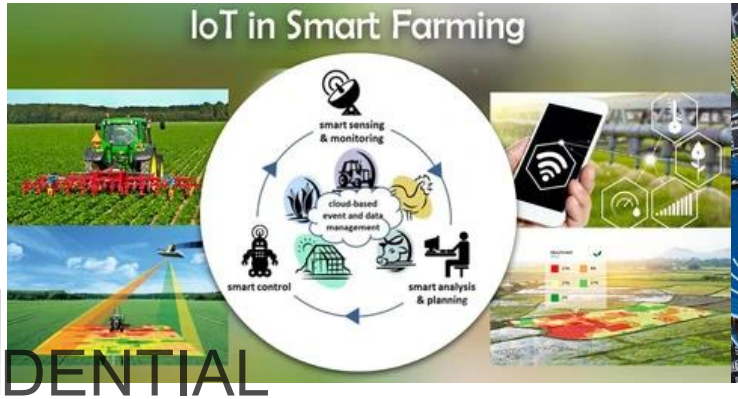
Industry Co-Development Center (ICC) with Industry Consortium for Next Gen Research and Workforce Development

Lead: Nihar Ranjan Mohapatra, Professor, EE, IIT Gandhinagar

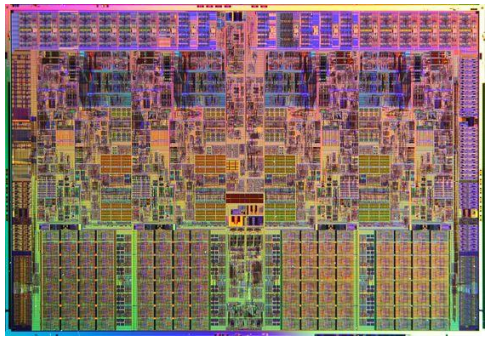
Co-Lead: Abhisek Dixit, Professor, EE, IIT Delhi

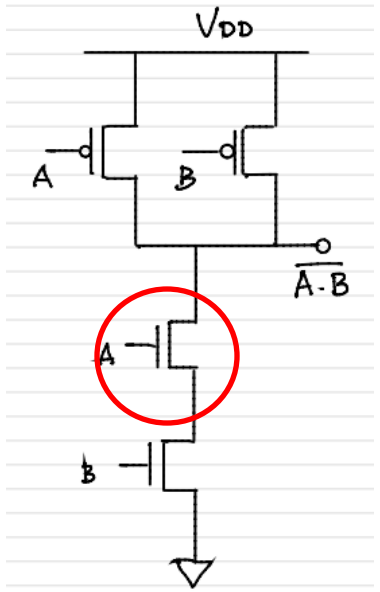
Life Runs on CMOS Technology

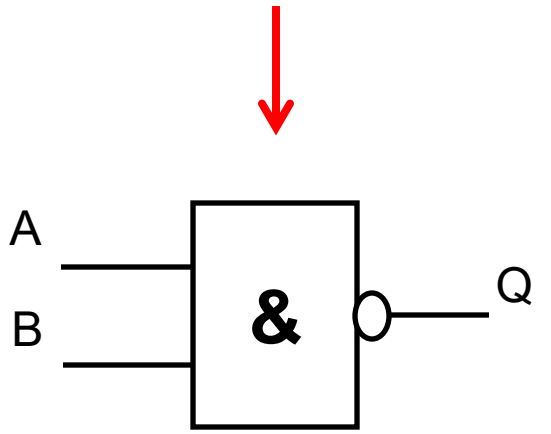




A Top-down view from an electronic product

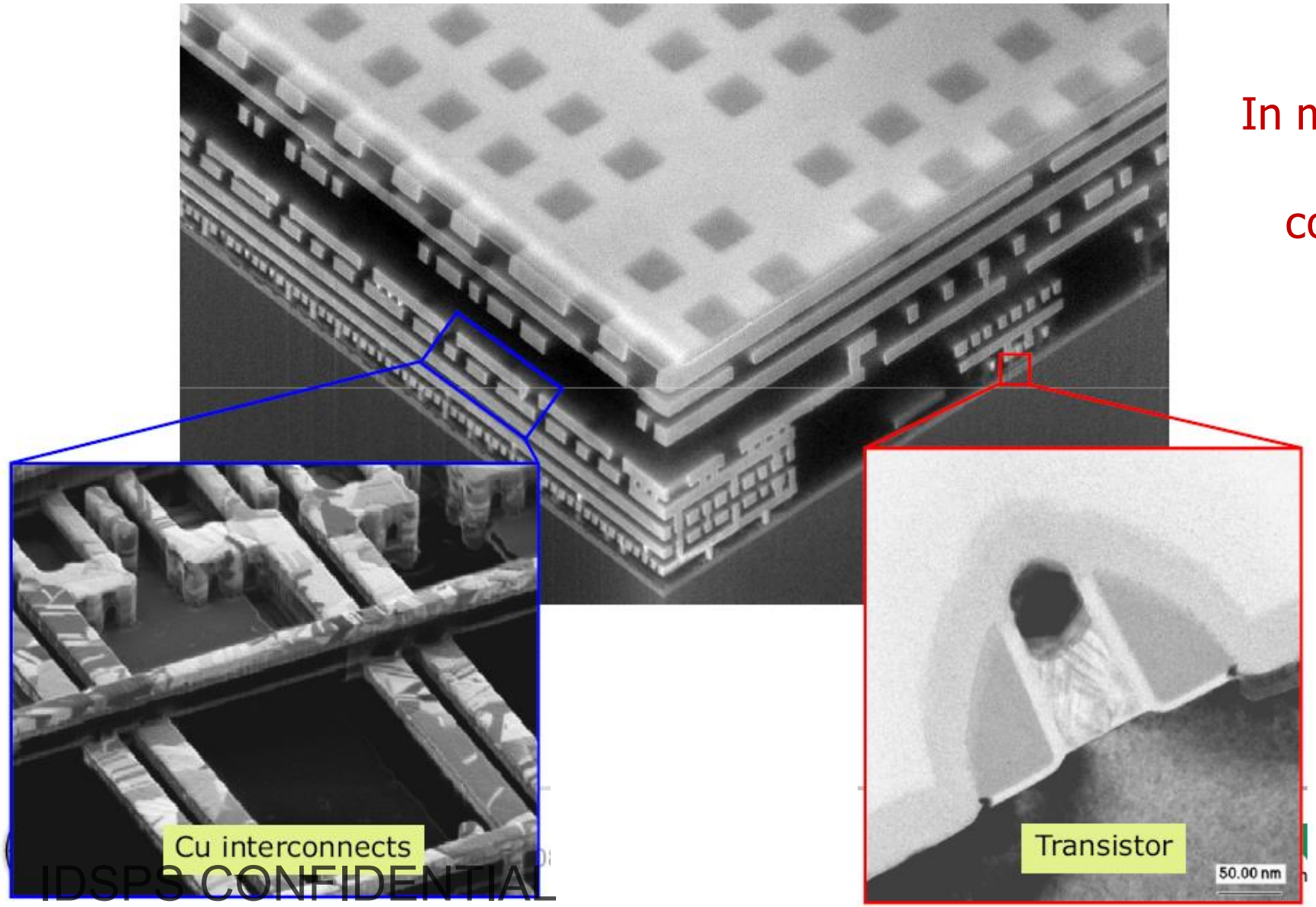






CMOS Devices are the basic components of any Integrated Circuit

Integrated Circuit (IC)

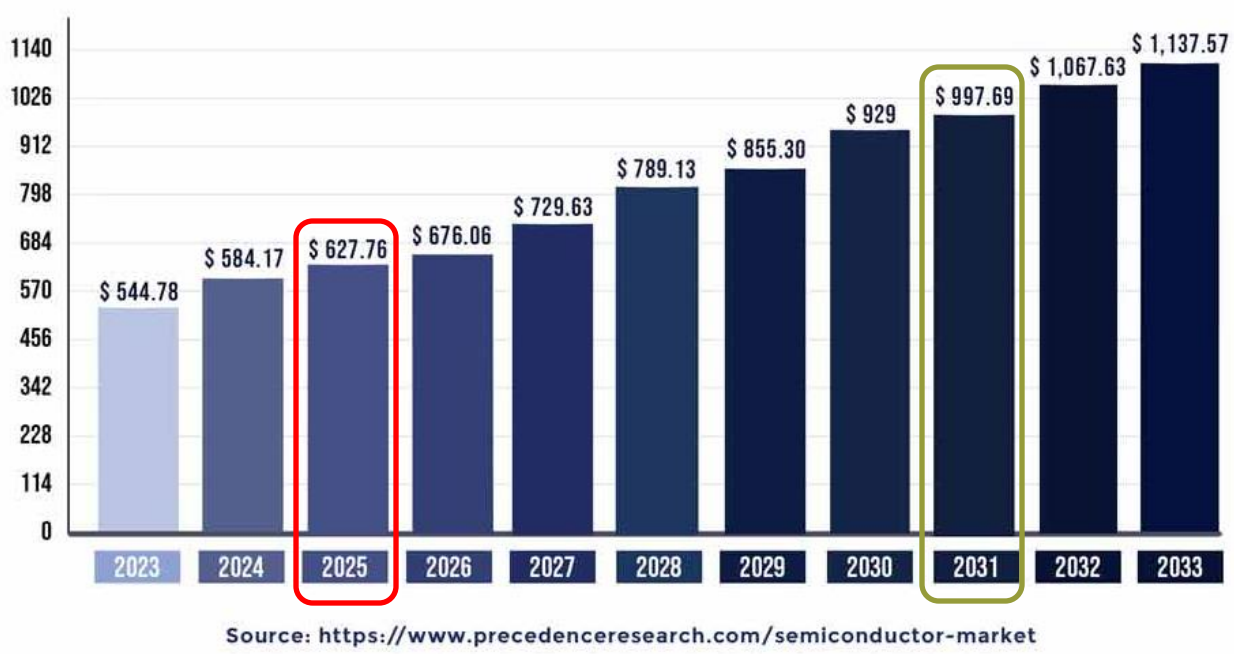


In modern day ICs, Billions of MOS devices are connected together by multiple layers of interconnects.

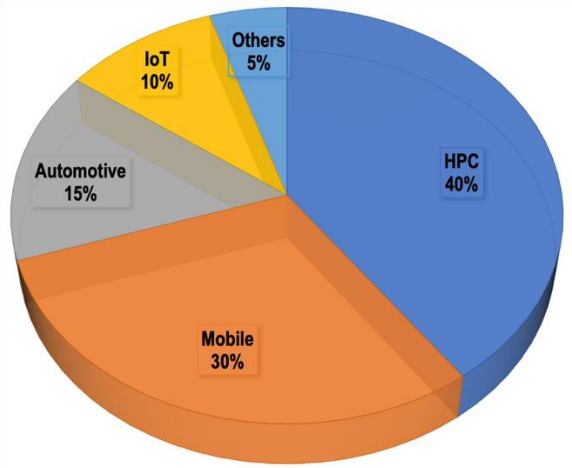
Market Trends

The global semiconductor market is booming

- Projected to grow from ~630 B$ in 2025 to ~1 T$ **by 2031**, at a CAGR of 14.9%



~$ 1 Trillion Market (2031)



Segment	Market %
HPC	40
Mobile	30
Automotive	15
IoT	10
Others	5

The advancement of CMOS technology (devices) in terms of power and performance are key for all these market segments

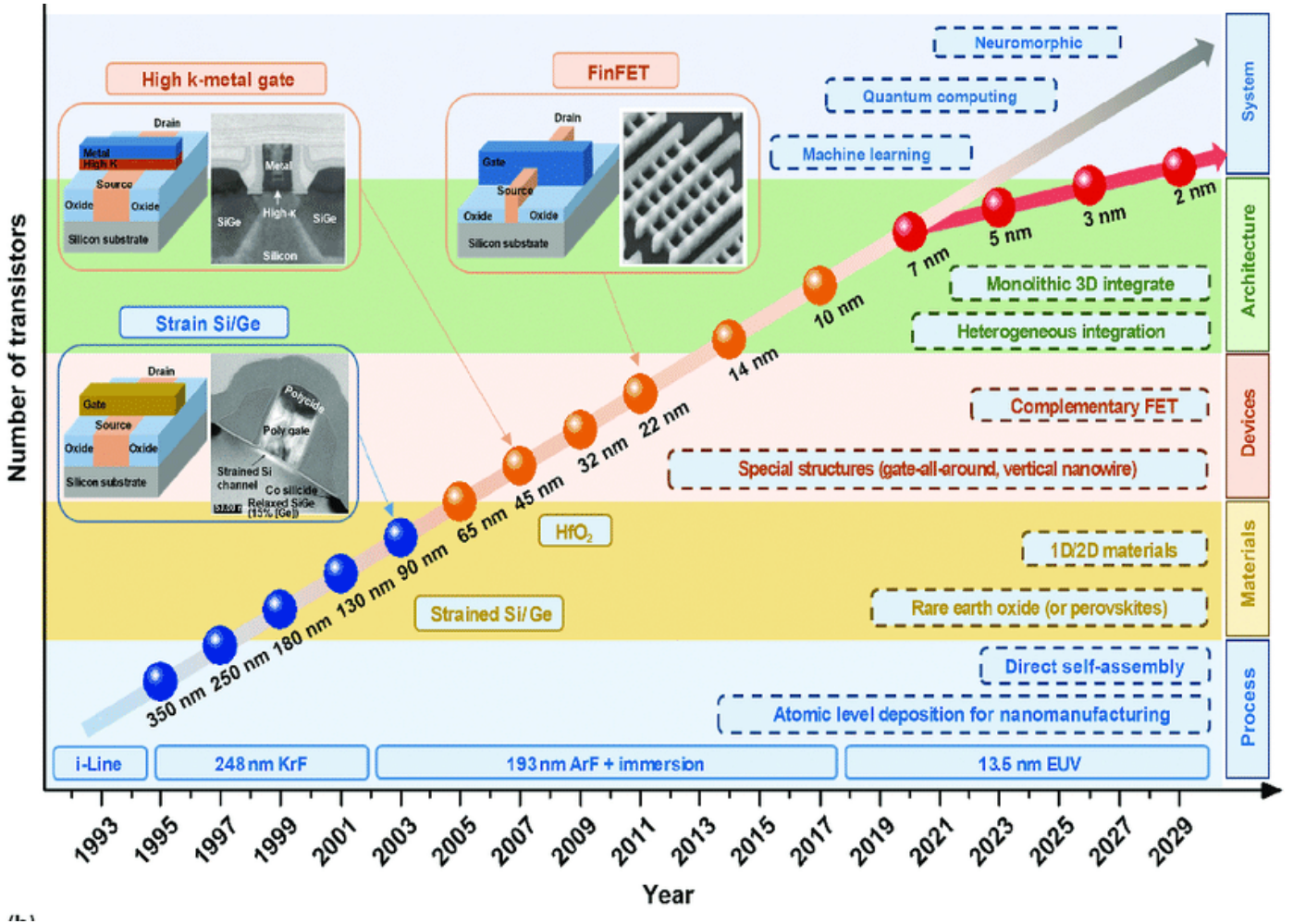
CMOS Technologies over the years

CMOS Technology Node		Year of Production
6 µm	N6000	1974
3 µm	N3000	1977
2 µm	N2000	1979
1.5 µm	N1500	1981
1 µm	N1000	1984
800 nm	N800	1987
600 nm	N600	1990
350 nm	N350	1993
250 nm	N250	1996
180 nm	N180	1999
130 nm	N130	2001
90 nm	N90	2003
65 nm	N65	2005
45 nm	N45	2007
32 nm	N32	2009
22 nm	N22	2012
14 nm	N14	2014
10 nm	N10	2017
7 nm	N7	2019
5 nm	N5	2021
3 nm	N3	2024
20 Å	N2	
15 Å	N1.5	
10 Å	N1	

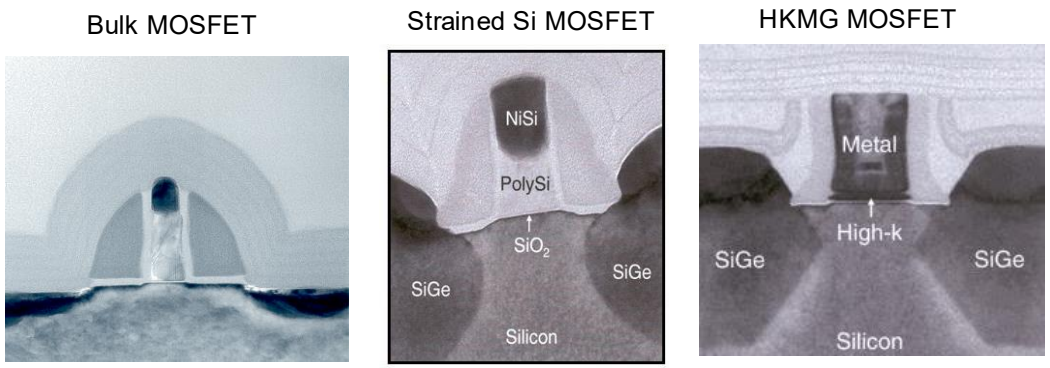
Traditional Scaling

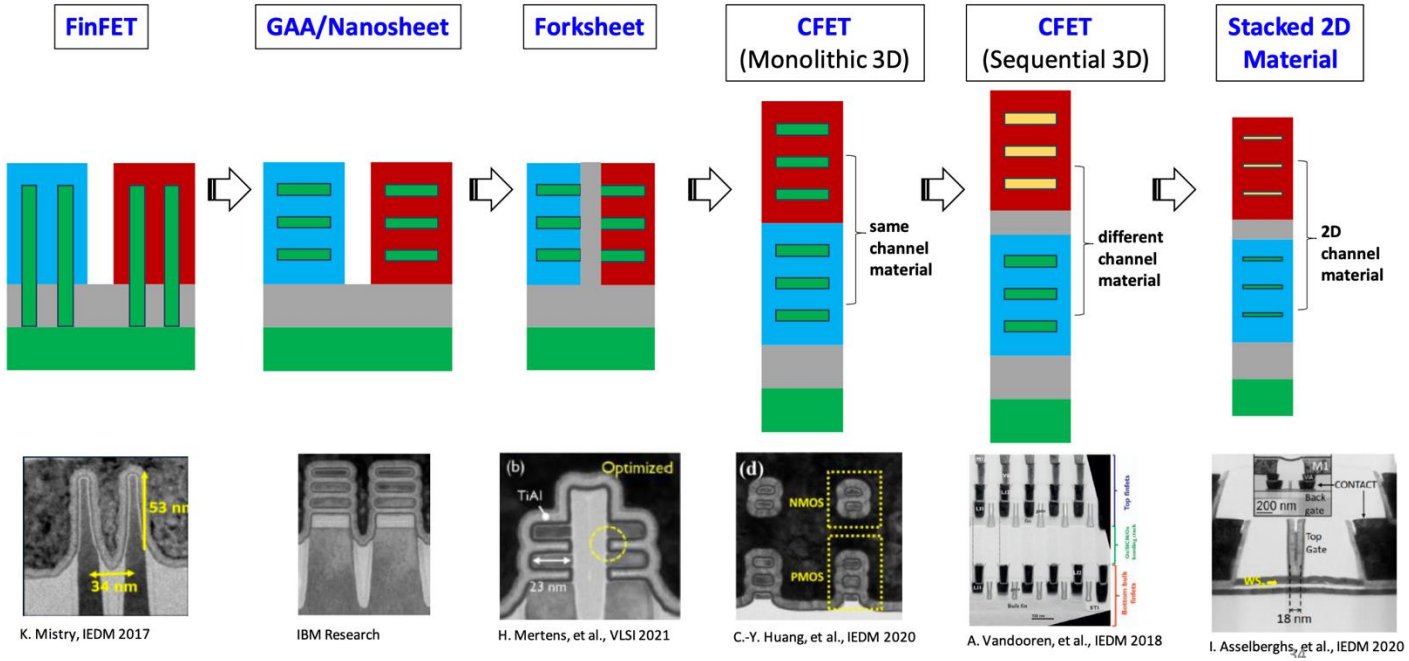
Equivalent Scaling

Footprint Scaling



Evolution of CMOS Transistors



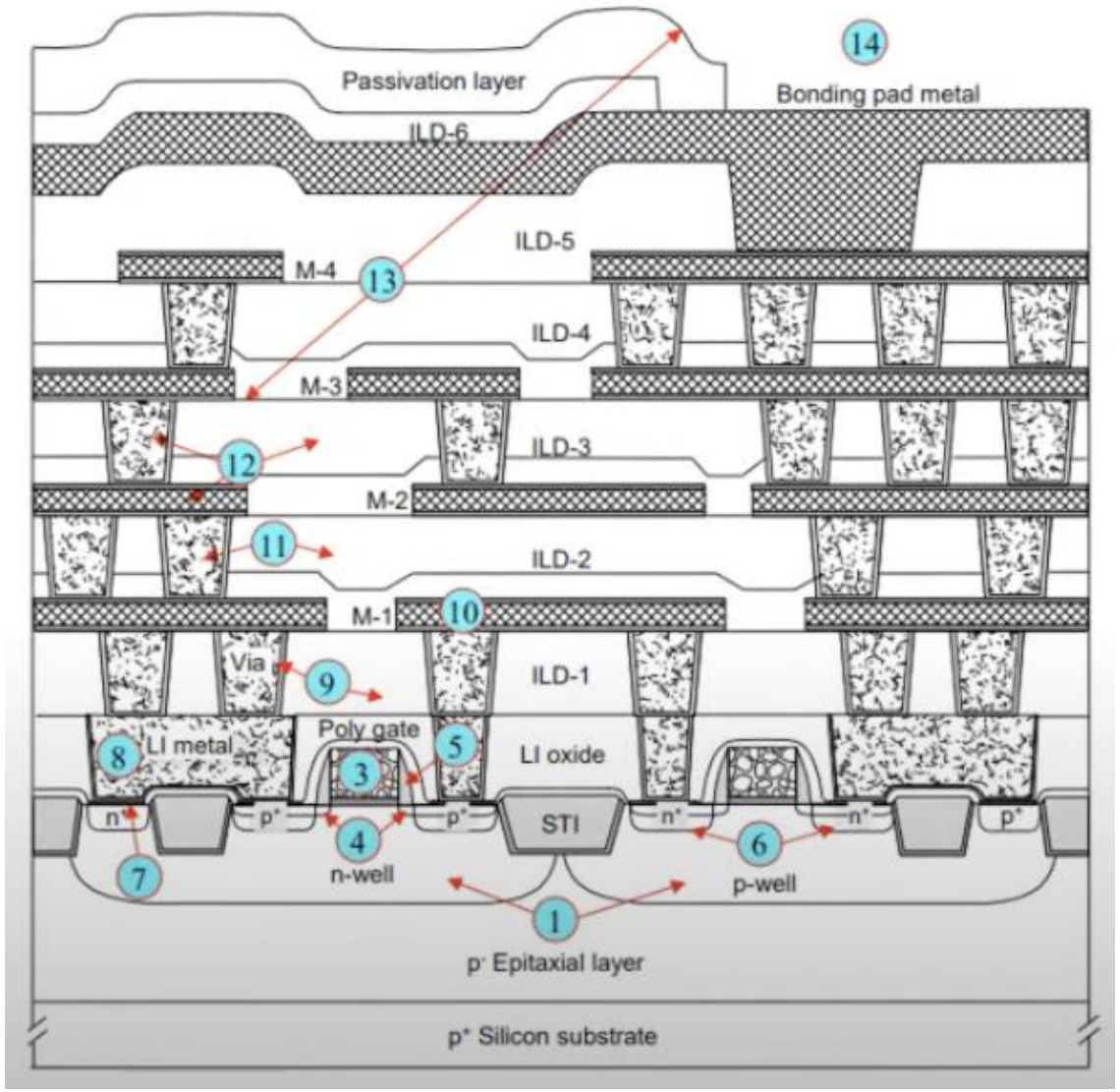


- Over the past 15 years, MOS transistors have evolved from traditional planar architecture to 3D architectures.
- The semiconductor industry is expected to transition from silicon as the primary material to alternatives like germanium and 2D materials such as MoS_2, WS_2, and WSe_2 in next 10 years.
- Additionally, the number of materials used in advanced technologies is increasing, which presents significant challenges for process integration and reliability.

Planar CMOS Technology – Process Flow and Process Steps

1970 - 2010

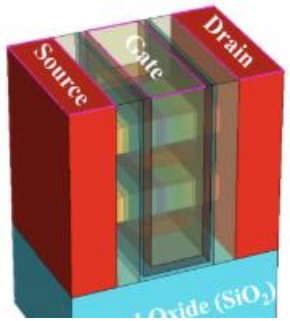
1. Ion Implantation (Wide Energy Range)
2. Dopant Diffusion / Activation
3. Epitaxial Growth
4. Etching (RIE, Wet)
5. Deposition (LPCVD, PECVD, HDPCVD, APCVD)
6. Oxidation (Dry, Wet)
7. Chemical Mechanical Planarization (CMP)



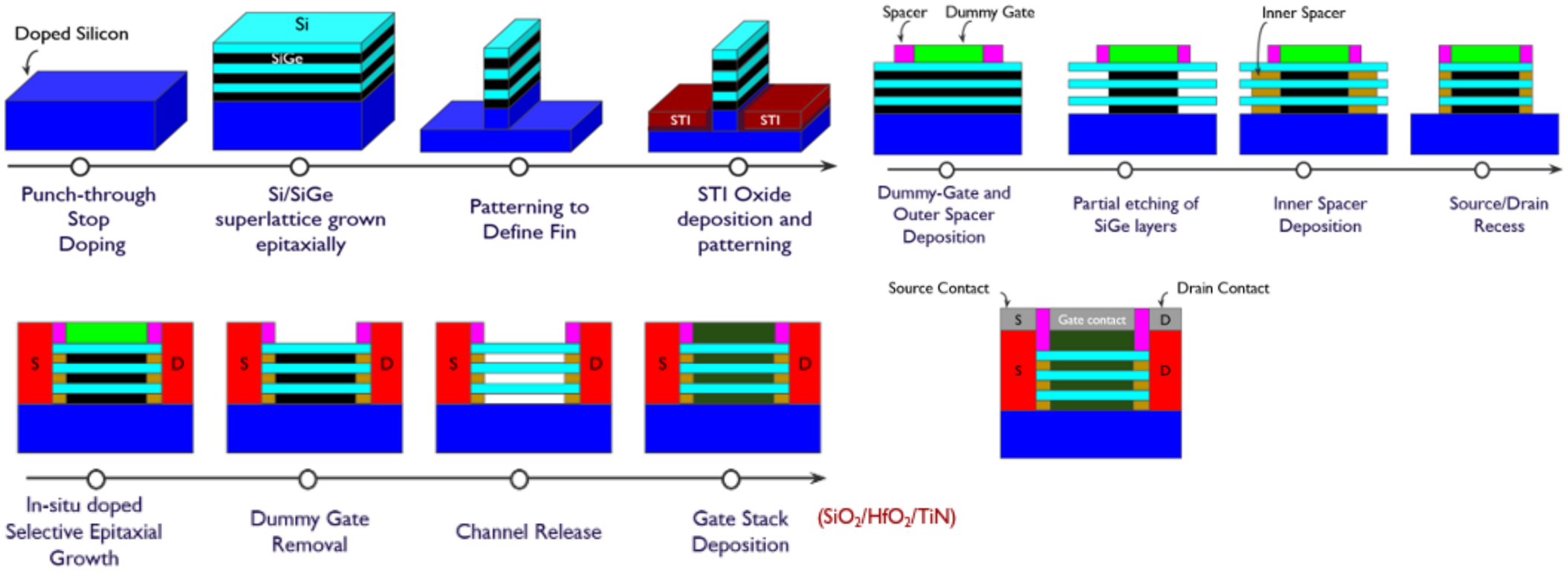
Typical Planar CMOS Process Flow

1. Twin-well Implants
2. Shallow Trench Isolation
3. Gate Structure
4. Lightly Doped Drain Implants
5. Sidewall Space
6. Source/Drain Implants
7. Contact Formation
8. Local Interconnect
9. Interlayer Dielectric to Via-1
10. First Metal Layer
11. Second ILD to Via-2
12. Second Metal Layer to Via-3
13. Metal-3 to Pad Etch
14. Parametric Testing

Next Generation Needs and Technical Challenges



NsFET

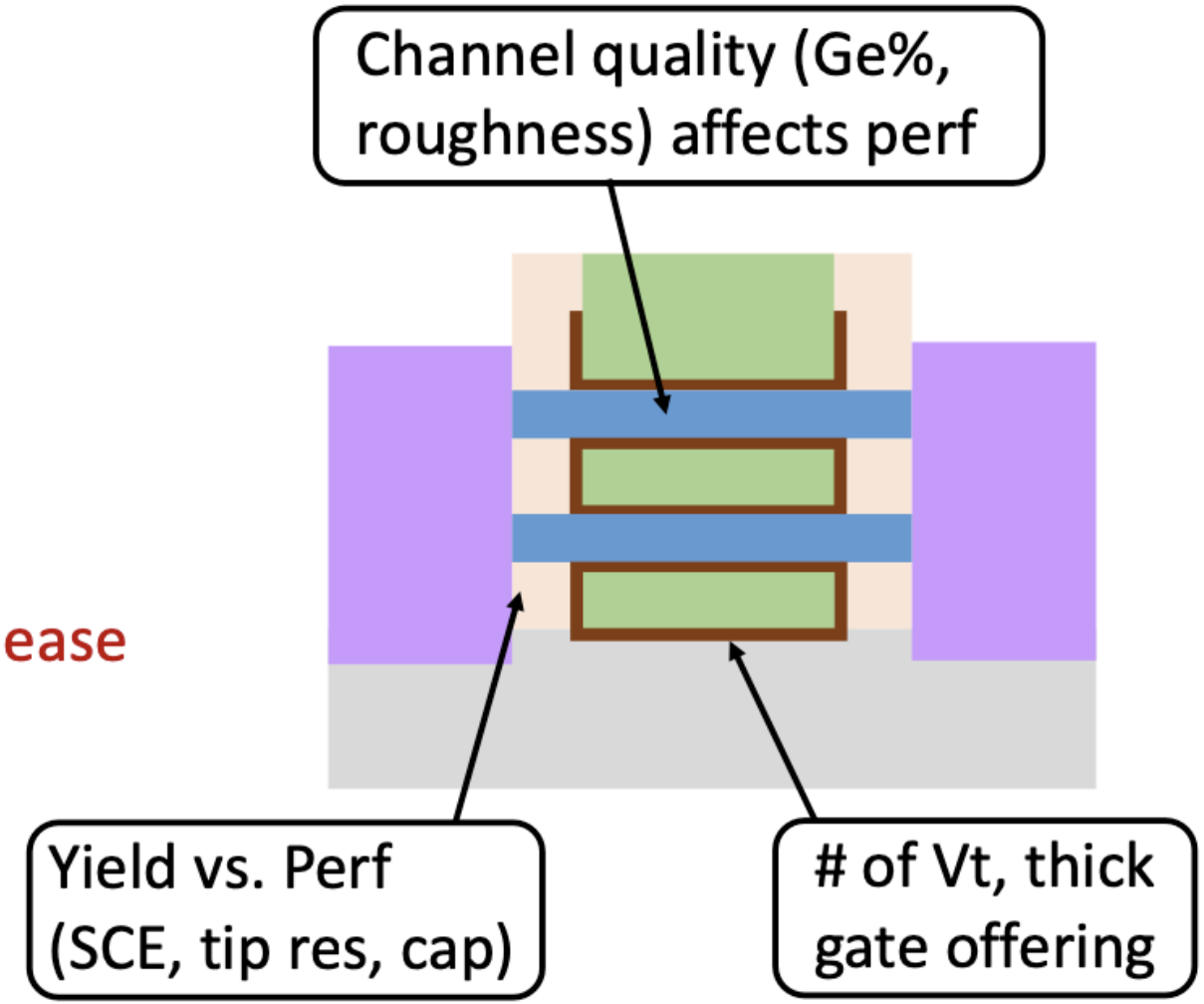


- An increasing number of process modules require critical etches and depositions based on ALD, ALE and other selective processes.
- Research and development in advanced materials, devices, and processes are essential to address the challenges posed by further scaling in CMOS technology.

Process Challenges

Generic Nanosheet FET Process Flow

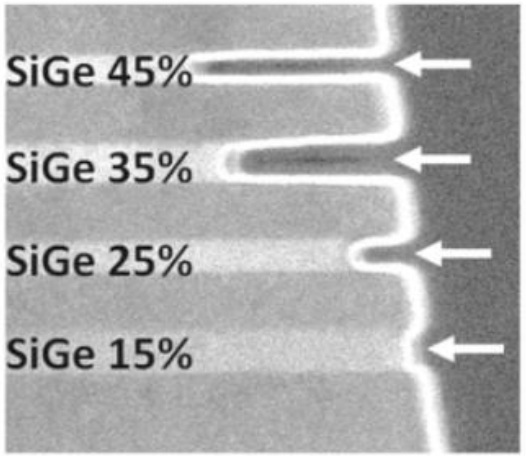
- Si/SiGe super-lattice stack
- Fin patterning, STI, fin reveal
- Dummy gate patterning
- Spacer formation and S/D epitaxy
- Dummy gate removal and channel release
- Gate Stack formation
- Contact formation



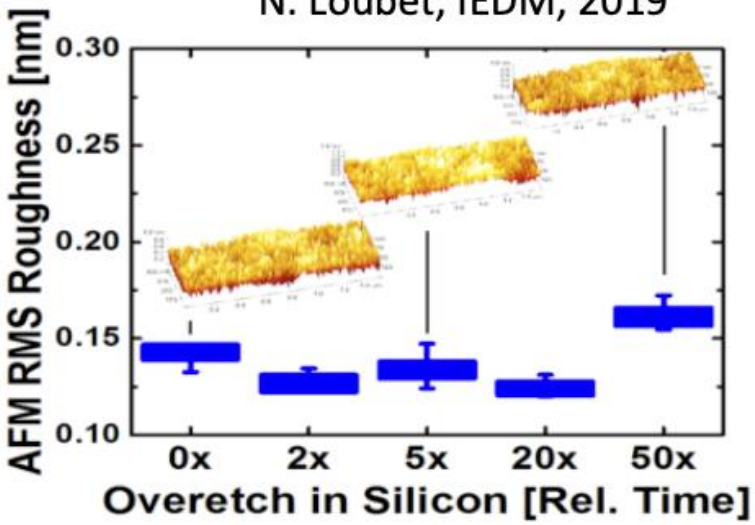
Process Challenges

More on nanosheet channel

- Ge% in SL affects Si channel purity, channel strain, inner spacer depth…etc.
- SL layer THK affects channel release, SCE, and drive

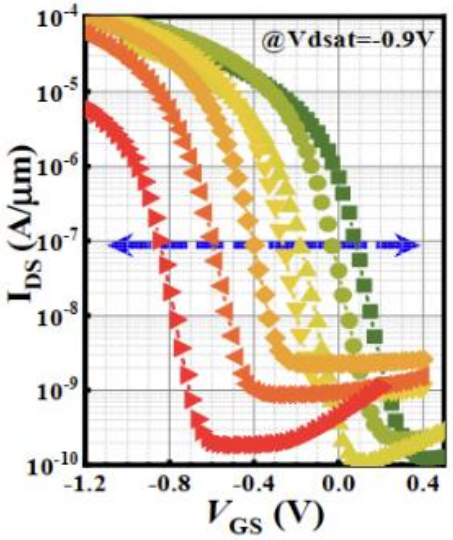


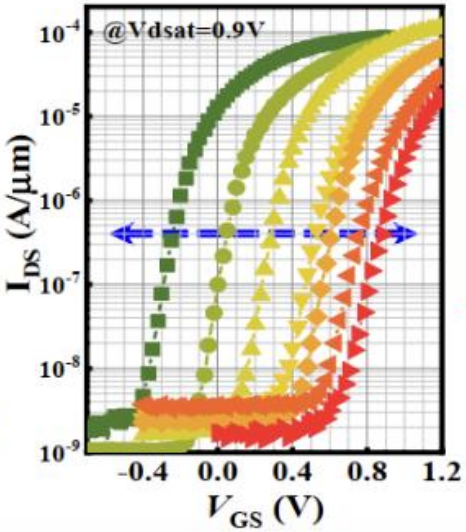
N. Loubet, IEDM, 2019

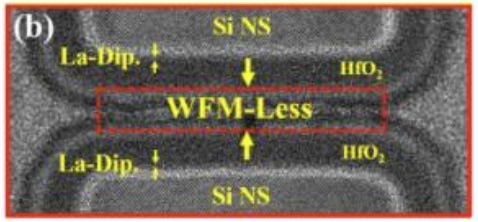


Vt control and offering

- Tight suspension space for Vt adjustment materials
- Seven Vt offerings by dipole has been demonstrated







J. Yao, IEDM, 2022

CMOS Devices ICC - Aim

To create a **transformative ecosystem** that drives innovation in CMOS devices and CMOS technology fueling sustainable manufacturing excellence in India through strategic collaborations with industry partners and academia

CMOS Device ICC - Objective

Next Generation CMOS Device ICC

Capability Building through Research and Innovation

Capacity Building through Skill Development and Academic Programs

Training and Research in the areas of

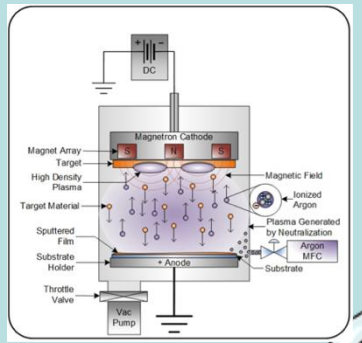
- Semiconductor Materials, Processes and Device Design
- Semiconductor Manufacturing
- IC Design

Strategic Research Focus Areas and Faculty Leaders

Semiconductor Processes:

Development
Modeling
Metrology

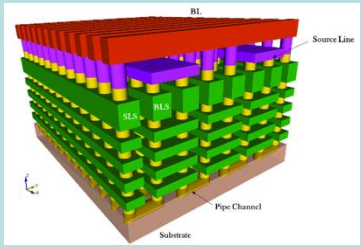
Nihar Ranjan Mohapatra (IITGn)
Sndip Lashkare (IITGN)
Anagh Bhaumik (IITGn)
Brajesh Rawat (IITRpr)
Ayan Roy Chowdhury (IITKgp)



Semiconductor Devices:

Next generation Logic Device
Next generation Memory Device
Modeling and PDK

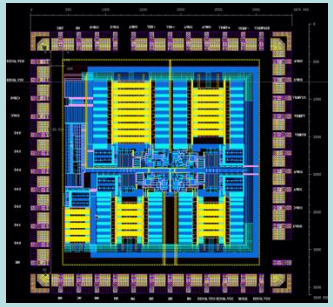
Nihar Ranjan Mohapatra (IITGn)
Sndip Lashkare (IITGN)
Abhisek Dixit (IITD)
Shubham Sahay (IITK)



Ankesh Jain (IITD)
Madhav Pathak (IITGN)
Nihar Ranjan Mohapatra (IITGn)

Integrated Circuits:

Logic Circuits
Analog/Mixed-Signal Circuits



Nihar Ranjan Mohapatra (IITGn)
Hari Ganesh (IITGn)
Rajesh Thakker (GTU)

Semiconductor Manufacturing:

AI Assisted Manufacturing
Advanced Process Control
Digital Twins

CMOS Device Core Team

Core Faculty Team

Nihar
EE, IITGN

Abhisek
EE, IITD

Sandip
EE, IITGN

Shubham
EE, IITK

Brajesh
EE, IITRPR

Ankesh
EE, IITD

Ayan
MSE, IITKGP

Anagh
MSE, IITGN

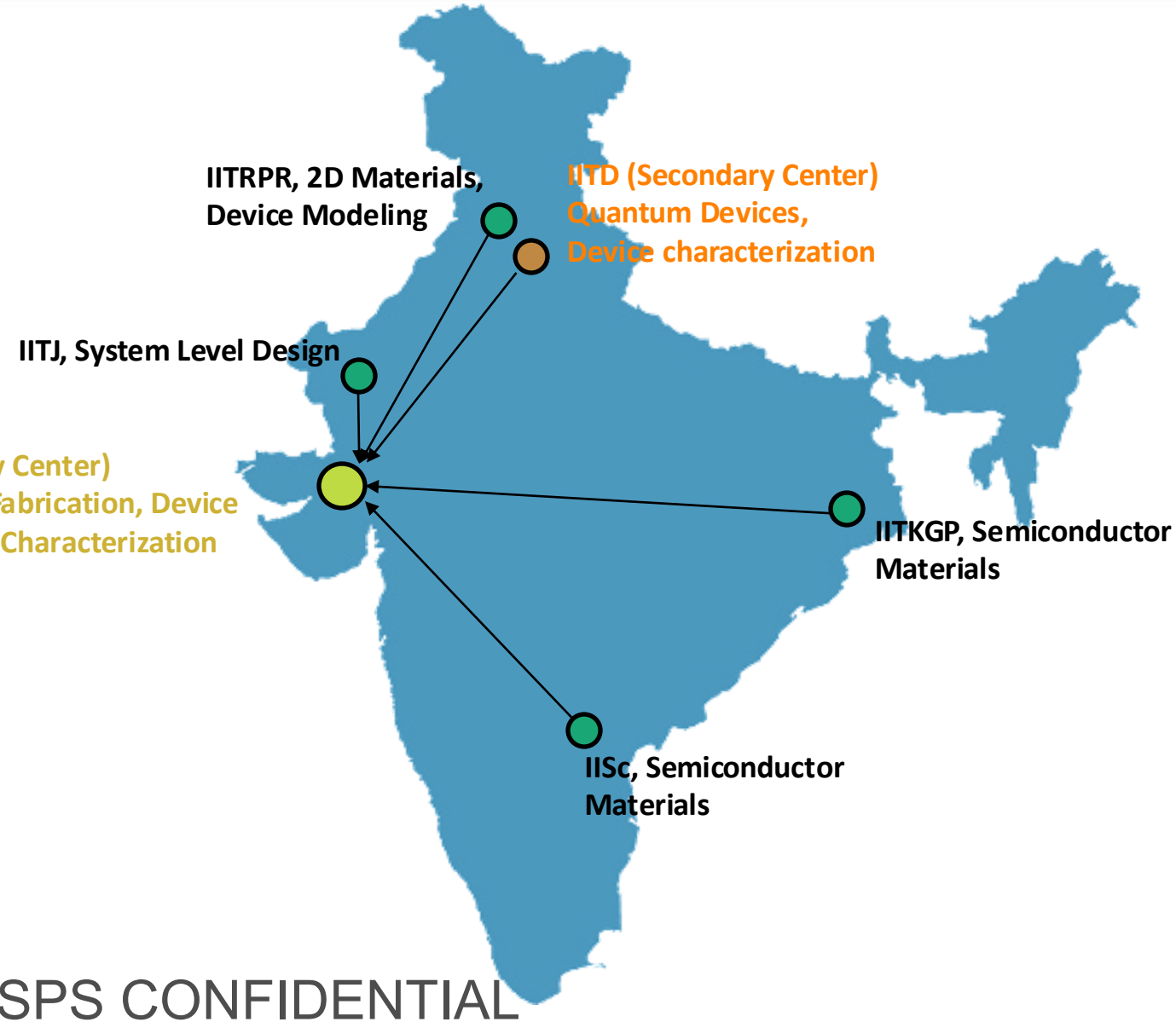
Cross-SRA Faculty with relevant expertise

Tarun Agarwal (EE, IIT Gn)
Predictive modeling and reliability

Bhagwati Prasad (MsE, IISc)
Materials

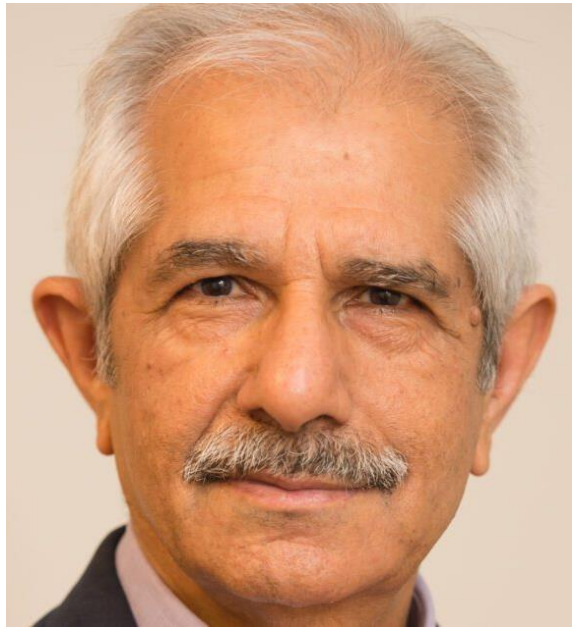
Binod Kumar (EE, IITJ)
System Design and Architecture

Primary and Satellite Centers



Engineering colleges of Gujarat and nearby states.

Global Academic Collaborators



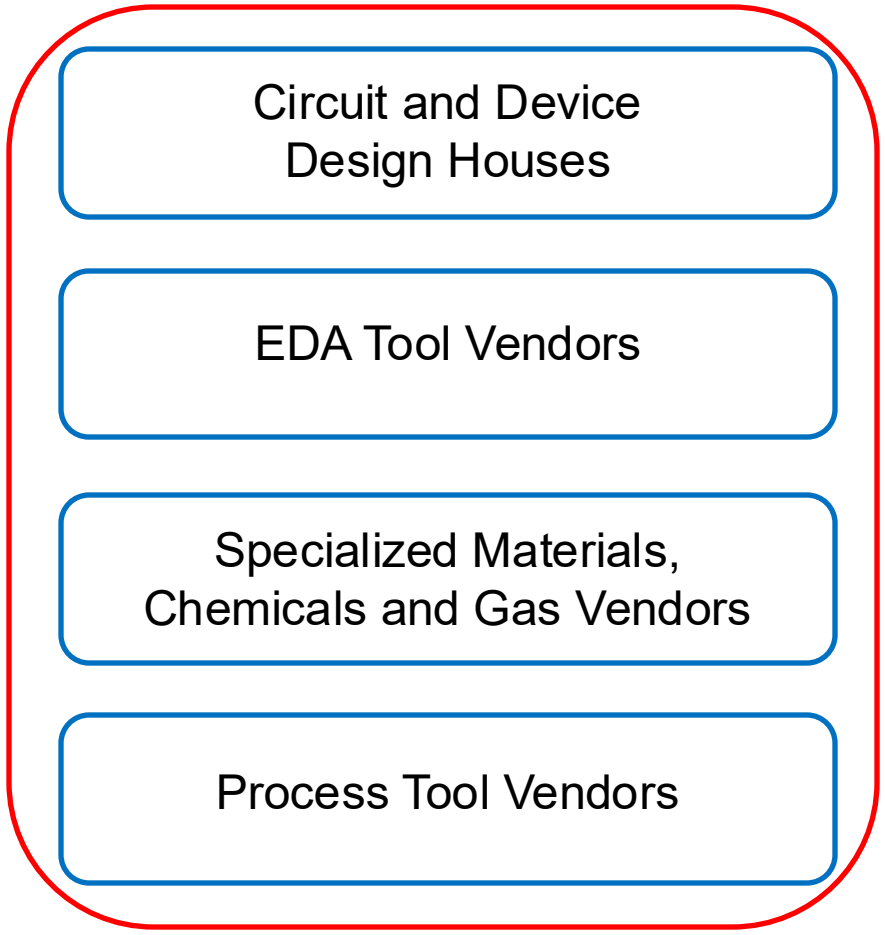
Prof. Rajendra Singh
D. Houser Banks Professor of Electrical and Computer Engineering
Clemson University

Prof. Suman Datta
Joseph M Pettit Chair of Advanced Computing
Georgia Research Alliance (GRA) Eminent Scholar
Professor
Georgia Tech.

Potential Industry Partners

Company	Location	Status	Research Area
Tata Electronics	India	Potential	Next generation CMOS Devices, CMOS Process Development, Process and Device Modelling, Device Characterization
Synopsys	India	Potential	AI assisted Device and Process Modelling, Digital Twin, Computational Lithography, Manufacturing and Yield
GlobalFoundries	USA and India	Potential	CMOS Devices, RFCMOS, Cryo-CMOS & Quantum Computing
Siemens EDA	India	Potential	Computational Lithography
Micron India	India	Potential	Memory Devices, Device Modelling
Western Digital	India	Potential	3-D NAND Flash Technology
Applied Materials	India	Equipment Supplier	Process Modelling, AI in Semiconductor Manufacturing
L&T Semi.	India	Potential	Quantum Computing, ASIC Design

Potential Industry Partners



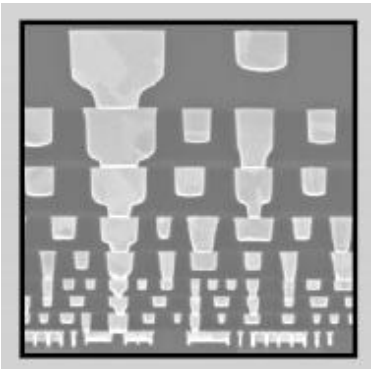
CMOS Devices ICC will work with all these companies to support them in their R&D and workforce development

Initial Research Projects with Faculty Leads

1. Optimizing HKMG Process for sub-3nm Stacked CMOS Technology (Lead: Nihar (IITGn))
2. Development of Specialized Materials and Devices for Cryogenic Applications in Quantum Computing and Space Electronics ((Leads: Abhisek (IITD), Anagh (IITGN))
3. Development of I/O and ESD devices for sub-10nm CMOS nodes (Lead: Sandip (IITGn))
4. Development of sub-1nm Stacked CMOS Technology using 2D Materials (Lead: Brajesh (IITRpr))
5. Next Generation Memory and Neuromorphic Computing with Resistive Switching Devices (Leads: Sandip (IITGn), Ayan (IITKgp) and Shubham (IITK))
6. Development of 2D Materials based Barrier Layer for BeoL Cu interconnects (Lead: Tarun (IITGn))
7. Resolution Enhancement Techniques for Lithography in Advanced CMOS Nodes (Lead: Nihar (IITGn))
8. Machine Learning Assisted Process-Device-Circuit Co-Optimization for Advanced CMOS Technologies (Lead: Nihar (IITGn))
9. Design of Analog Circuits using Semi-Supervised Graph Machine Learning (Lead: Ankesh (IITD))
10. Digital Twins in Semiconductor Manufacturing (Lead: Nihar (IITGn), Rajesh (GTU))

Required infrastructure

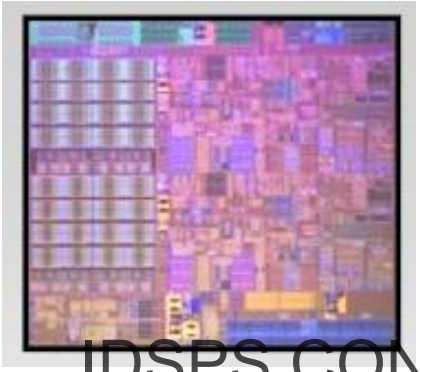
Optical Lithography



Thin Film Deposition and Etch

Ion Implantation and Anneal

Thermal Oxidation



CMP and Electroplating

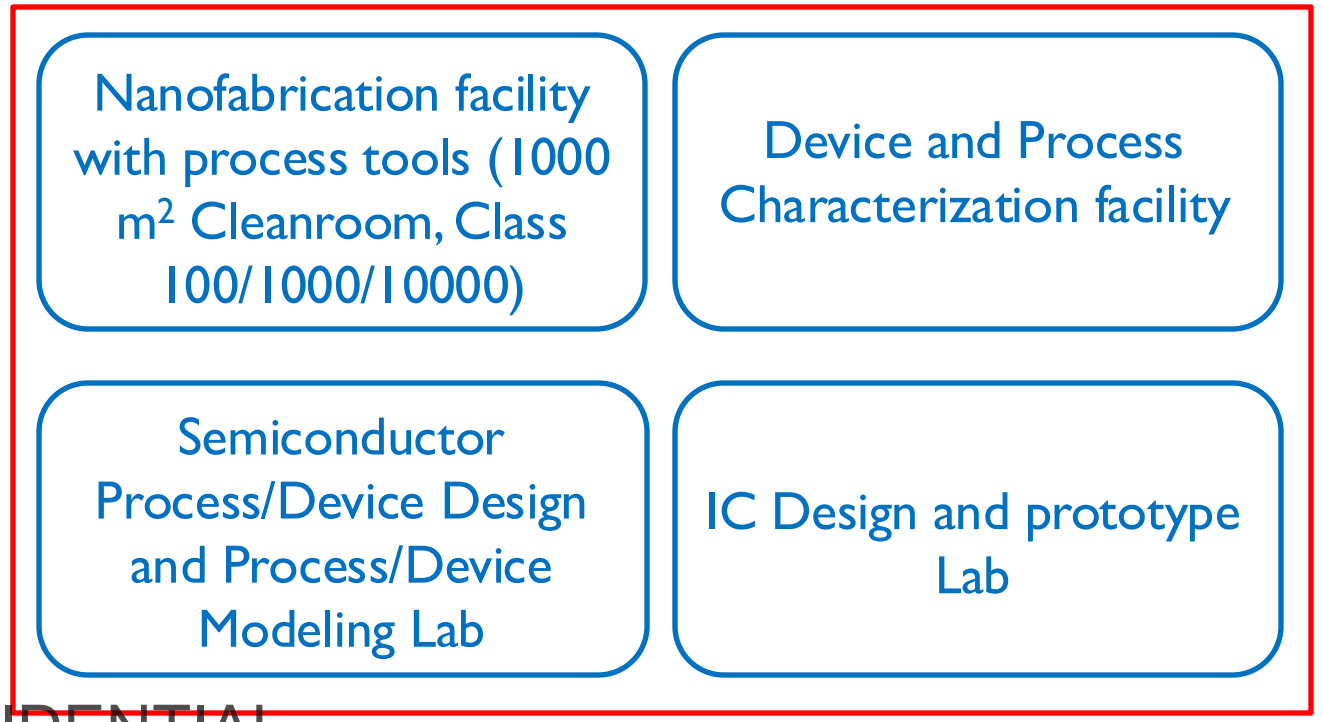
Process and Device Characterization

- Class 100, 1000 and 100000 cleanrooms
- Utlities required for the tools

- Ebeam Lithography
- Mask Aligner
- Resist Track System
- Oxidation Furnaces
- PECVD
- PALD
- Sputtering Systems for Dielectrics and Metal
- RIE
- Wet Benches
- Plasma Implanter
- RTA tools
- In line SEM
- Stress and adhesion measurement systems
- ESD characterization setup
- Parametric Analyzers and Probe Cards

Silicon and Advanced Semiconductor MAnifacturing Research and Training Hub (SAMARTH (समर्थ))

A centralized hub for research and ecosystem development in the areas of Semiconductor Process and Device Design, Process Technology and IC Design



Five Year Milestone

Milestones	Year 1	Year 2	Year 3	Year 4	Year 5
Submit Proposal					
Identify industry partners					
Set up industry consortium					
Set up infrastructure					
Develop Research Programs					
Develop Educational Programs					
Demonstrate Technologies					
Integrate Technologies into Industry Prototype 1					
Integrate Technologies into Industry Prototype 2					
Integrate Technologies into Industry Prototype 3					

Educational Plan (CMOS Device ICC)

- New Academic Programs in Semiconductor
- Skilling the workforce in local engineering colleges
- Train the Trainers (Upskilling Engineering Faculty)
- Certificate Courses for upskilling Industry Practitioners
- Workshops and Summer Camps for enhancing awareness among youths

Deliverables – Workforce Development Programs

Capacity Building Programs	# Output					
	Year 1	Year 2	Year 3	Year 4	Year 5	Total
Undergraduate	50	50	100	150	150	500
Postgraduate (MTech)	20	40	60	80	100	300
PhD	5	5	10	10	20	50
Upskilling – Engineering Faculty (Train the Trainer)	50	50	50	50	50	250
Upskilling – Industry Professionals	50	50	50	50	50	250
Certificate Courses	100	100	200	300	300	1000
Summer School	50	50	50	50	50	250

THANK YOU

Development of Specialized Materials and Devices for Cryogenic Applications in Quantum Computing and Space Electronics

Lead: Abhisek Dixit (IIT Delhi), Anagh B (IIT Gandhinagar)

Objective: To develop specialized materials and fabricate ultra-scaled devices for quantum, space, and cryogenic applications. These devices will be integrated with commercial silicon CMOS platforms, followed by comprehensive characterization and modelling at cryogenic temperatures.

Parameter	Current Status	Proposed
Architecture	Sub-7nm CMOS	Quantum bits integrated with cryo-CMOS based controller
Application	Digital logic	Quantum Computing & Space
Elements	HfO2 (ALD) + TiN (MOCVD) + Ni(Pt)Si + e-SiGe S/D	Gate stack and silicide material scanning, S/D engineering with SiGe for advanced transistors and quantum bits

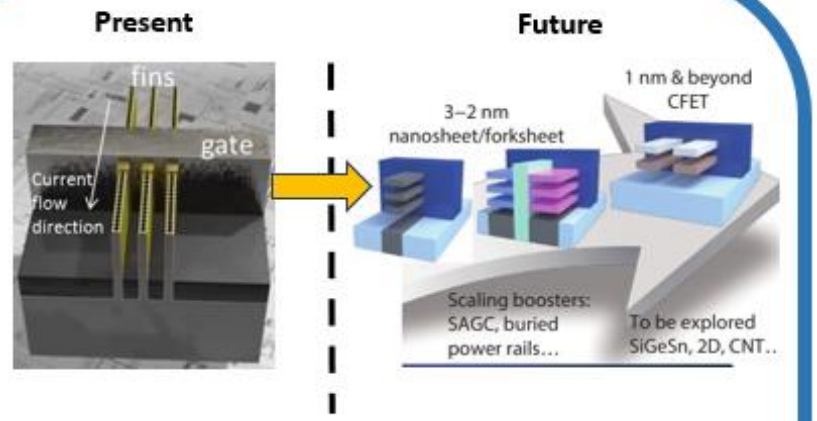


Fig. (A): Logic devices: from 7-nm FinFETs (left) towards 5-nm and beyond using lateral and vertical GAAFETs (right)

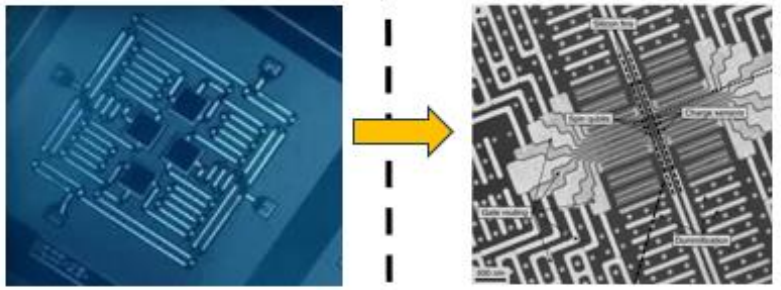


Fig. (B): Quantum Computing: from superconducting (left) to semiconducting qubits (right) with on-chip integrated cryogenic CMOS based control to achieve beyond NISQ computer

1. **Bao et al., "High Performance Nanosheet Technology Optimized for 77 K," IEDM 2023. (IBM)**
2. **Zwerver *et al.*, Qubits made by advanced semiconductor manufacturing. *Nat Electron* 5, 184–190, 2022. (Intel)**

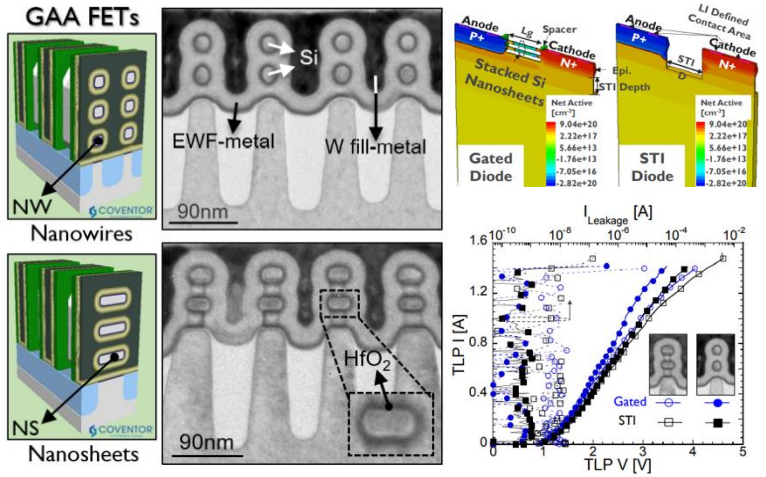
Development of I/O and ESD Devices for Sub-10nm CMOS Nodes

Lead: **Sandip Lashkare (IIT Gandhinagar), Nihar Ranjan Mohapatra (IIT Gandhinagar)**

Objective: Development of on-chip electrostatic discharge protection devices for advanced technology CMOS nodes.

Outcome: Designs for ESD protection devices for advanced CMOS nodes

	Prior Art	Proposed
Application	Low Speed Interfaces	High-speed Interfaces
Technology	GAAFET	GAAFET, CFET
Failure Currents	Low	High
Capacitance	High	Low



Approach

3D TCAD based Process Development: Calibration and Optimization with the latest technology nodes

Device Design: High current vs Capacitance trade-off analysis for device geometry

Integration: Device unit Processes and Geometry integration to increase failure current and decrease capacitance

Testing: Unit device testing for ESD models

- S. -H. Chen *et al.*, "ESD Protection Diodes in Sub-5nm Gate-All-Around Nanosheet Technologies," *2020 EOS/ESD Symposium*
- 'Next to FinFET, how will ESD suffer?', ESD Association, 2021

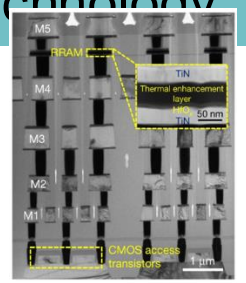
Next Generation Memory and Neuromorphic Computing with Resistive Switching Devices

Lead: Sandip Lashkare (IIT Gandhinagar), Co-Leads: Shubham Sahay (IIT Kanpur), Ayan Roy Chowdhury (IIT Kharagpur)

Objective: To develop CMOS-compatible materials for a Resistance Random Access Memory and their integration with advanced CMOS technology nodes for neuromorphic computing and hardware security applications

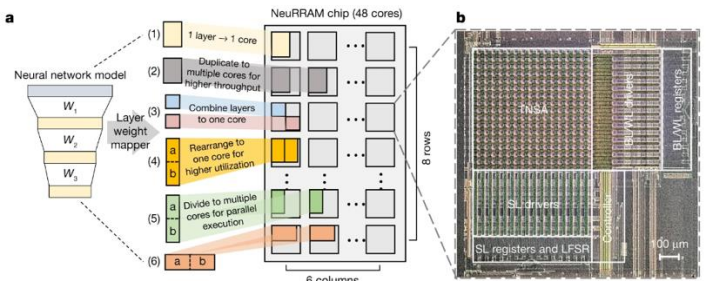
Outcome: Integration of RRAM with CMOS Technology

	Prior Art	Proposed
Technology	14nm	<10nm
Material	HfO_x	TiOx/HfOx, Si:HfO_x
Variability	High	Low



Synapses

Neurons



Approach

Technology Development

CMOS compatible Materials Developments:
Low variability, Low temperature processes unit HfOx-RRAM for synapse

Synapse Array: RRAM-Synapse array (Learning Block)

Integration: Unit HfOx RRAM Integration with CMOS Neuron

Complete Neuromorphic Computing System:
HfOx RRAM array and CMOS Neuron Network

- Wan, W. *et al.* A compute-in-memory chip based on resistive random-access memory. *Nature* (2022)
- R. K.-Aljameh *et al.*, "HERMES Core – A 14nm CMOS and PCM-based In-Memory Compute Core using an array of 300ps/LSB Linearized CCO-based ADCs and local digital processing," *2021*

Development of Stacked CMOS Technology using 2D Materials

Lead: Brajesh Rawat (IIT Ropar), Co-Leads: Ayan Roy Chowdhury (IIT Kharagpur)

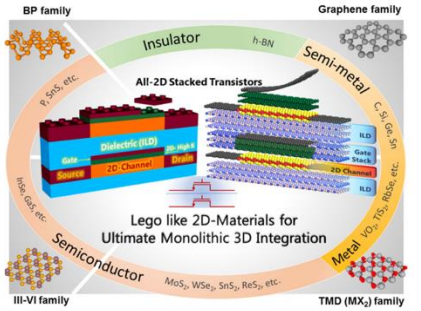
Objective: To develop Si-compatible 2D material-based MOS Transistors with a focus on enhancing speed and energy efficiency. Additionally, design novel 3D CMOS architectures, such as FSH and CFET, using 2D materials for future technology nodes.

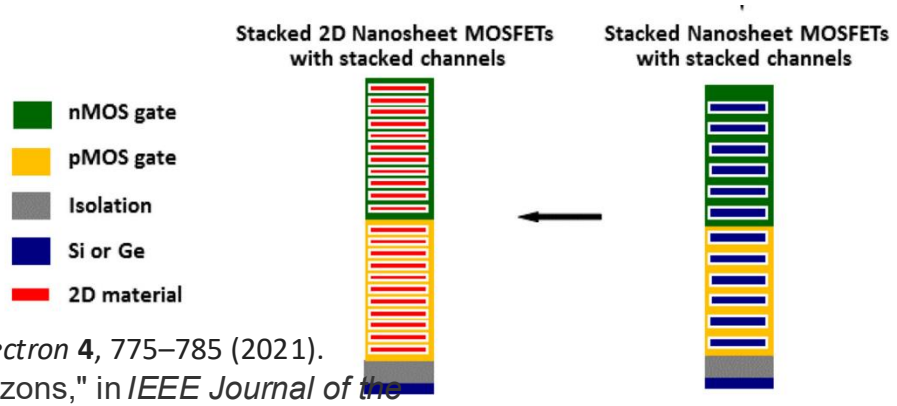
Parameter	Current Status	Proposed
Doping and Contact Resistance	Challenges in precise doping control and high contact resistance.	Innovate doping techniques to develop Si compatible devices.
Fabrication Complexity	High complexity in multilayer alignment and integration of 2-D materials.	Develop precision alignment and stacking techniques for reliable multilayer 2-D material integration
Reliability issues	Interfacial traps, fabrication defects and thickness non-uniformity affecting performance	Focus on defect and trap management strategies and scalable fabrication processes to improve yield and device scaling.

Outcome:

2-D material based devices optimized for speed, energy efficiency and scalability

A scalable and reliable 3-D CMOS technology using 2-D materials by addressing challenges in doping, contact resistance, thermal management, and device uniformity.



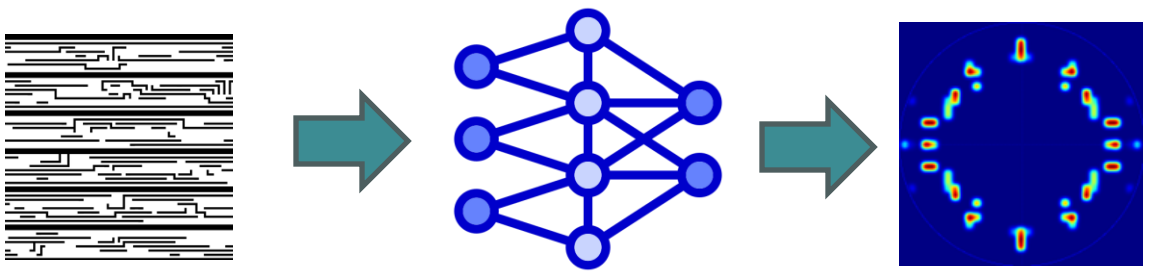


- Zhu, K., Wen, C., Aljarb, A.A. *et al.* The development of integrated circuits based on two-dimensional materials. *Nat Electron* **4**, 775–785 (2021).
- F. Schwierz and M. Ziegler, "Six Decades of Research on 2D Materials: Progress, Dead Ends, and New Horizons," in *IEEE Journal of the Electron Devices Society*, vol. 10, pp. 443-451, 2022,

Source Mask Optimization for Lithography in Advanced Nodes

PI: Nihar Ranjan Mohapatra (IIT Gandhinagar)

Objective - Develop an Active Sampling based Machine Learning model that can directly generate optimized source for given layout clips to achieve simulation speed up of about 10^4 times



Approach

- Generating Dataset
- Active Sampling
- ML Model Training
- Optimized Source

Proposed vs. Prior Art

	Current State	Proposed
Simulation Time	~ 1-4 hours	~ few seconds

Outcome and Impact

- An efficient and fast ML based Source optimization framework for SMO in lithography for advanced technology nodes
- Faster and efficient optimization of lithography process in semiconductor chip manufacturing

References*

1. Ahmed A. Alkrush, Mohamed S. Salem, Osama. Abdelrehim, A.A. Hegazi, Data Centers Cooling: A Critical Review of Techniques, Challenges, and Energy Saving Solutions., International Journal of Refrigeration (2024).
2. COOLERCHIPS: Cooling Operations Optimized for Leaps in Energy, Reliability, and Carbon Hyperefficiency for Information Processing Systems, Advanced Research Projects Agency – Energy, U.S. Department of Energy (2023).

Machine Learning Assisted Process-Device-Circuit Co-Optimization for Advanced CMOS Technologies

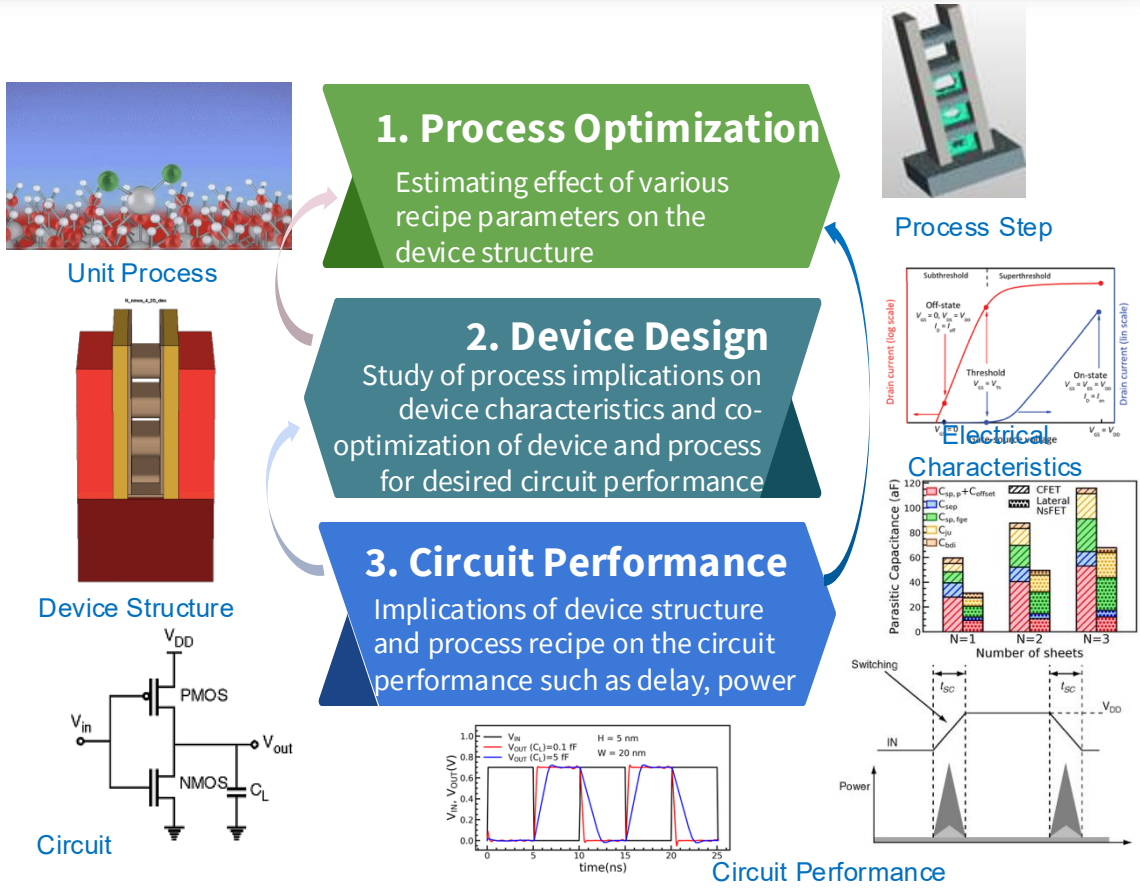
PI: Nihar Ranjan Mohapatra (IIT Gandhinagar)

Objective: To develop a machine learning-assisted framework for co-optimization of process parameters, device characteristics, and circuit performance in advanced CMOS technologies, enabling more efficient and effective design and manufacturing processes.

Challenges in CMOS Scaling: Increasing complexity in design and fabrication at smaller nodes
Traditional Methods: Sequential optimization of process, device, and circuit leads to suboptimal outcomes and higher costs
ML Advantages: Provides a holistic approach to identify optimal parameters across different design levels simultaneously

Technical Approach:

- Emulate effect of various process parameters on device structure in feature-scale process simulators.
- Device structure from the process model is simulated for electrical characteristics and parasitic capacitances
- Device structural and electrical parameters are used to predict circuit performance parameters such as delay and power
- The ML models at the three stages are inter-weaved for co-optimization



Proposed vs. Prior Art:

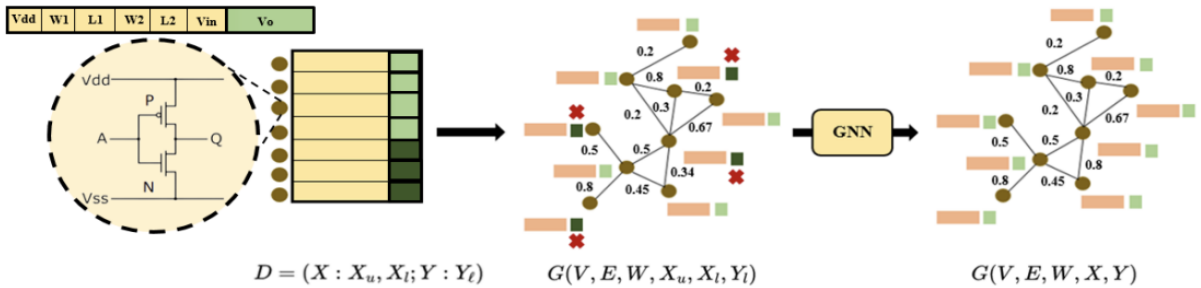
	Current State	Proposed ML Approach
Simulation Time	~ 4-8 hours	~ few seconds

Design of Analog Circuits using Semi-Supervised Graph Machine Learning

PI: Ankesh Jain (IIT Delhi)

Objective: To design analog circuits with the help of machine learning

Outcome: A crucial initial step towards the automation of Analog circuit design, promising more efficient design cycles and groundbreaking advancements in the field.



Miller Compensated Two-stage OTA (Optimization)

Objective: Minimize FOM st. Gain > 50 dB ; UGB > 100 Mhz ; PM > 45 deg ; GM > 15 dB ; Power < 900 μW ; Noise < 600 nVrms

Model	Gain (dB)		UGB (MHz)		GM (dB)		PM (deg)		Noise (nV)		Power (μW)		Success
(specs)	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	(out of 10)
DE [24]	58.6	53.3	190	165	19.2	17.8	46.7	45.0	478	463	815	633	04/10
BO-EI[1]	**68.3**	65.6	**225**	190	18.9	17.8	**52.0**	45.6	470	462	627	505	03/10
EASCO	67.3	64.4	**215**	192	**19.2**	18.5	47.2	45.5	470	**462**	722	**490**	**04/10**
ASTROG	**80**	61.6	145	106	**26**	23.5	**52.5**	47.9	497	**446**	716	**318**	**06/10**

Approach:

Graph of Circuits: circuit instances are encoded as nodes within a graph.

Graph-Based Surrogate Model: graph-based surrogate model, employing a semi-supervised learning framework acts as a valuable proxy for SPICE simulations, significantly reducing the dependence on extensive labelled datasets.

Optimization Algorithms: efficient Analog Sizing via Constrained Optimization (EASCO) and Analog Sizing through Real-time Online Graphs (ASTROG), which ensures optimal design parameters that align with the designer's criteria.

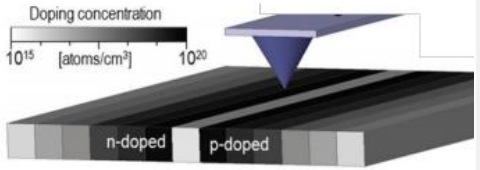
1. *A. Shahane, S. Manjiri, A. Jain and S. Kumar, "Graph of circuits with GNN for exploring the optimal design space", 36th Advances in Neural information processing systems (NeurIPS), 2023, New Orleans.*
2. Samrat L. Sabat, K.Shravan Kumar, and Siba K. Udgata. Differential evolution and swarm intelligence techniques for analog circuit synthesis. In 2009 World Congress on Nature Biologically Inspired Computing (NaBIC), pages 469–474, 2009
3. Shady A. Abdelaal, Ahmed Hussein, and Hassan Mostafa. A bayesian optimization framework for analog circuits optimization. In 2020 15th International Conference on Computer Engineering and Systems (ICCES), pages 1–4, 2020.

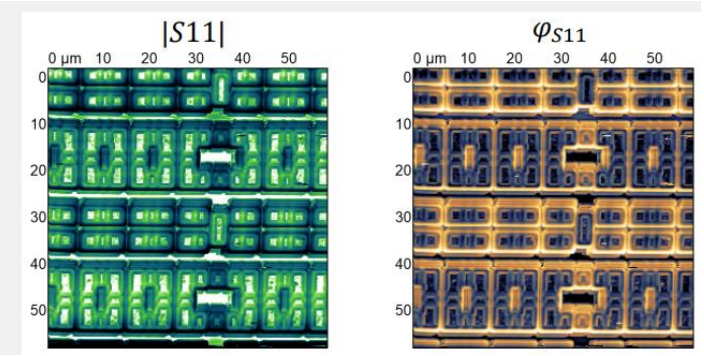
Nanoscale AFM based characterization of CMOS reliability analysis

PI: Nityanand Gosvami (IIT Delhi)

Objective: To establish nanoscale characterization based on atomic force microscopy techniques to determine various modes of failure including leakage paths in the circuits, structural inaccuracy, mapping of dielectric properties and doping density with nanometer precision

Approach:

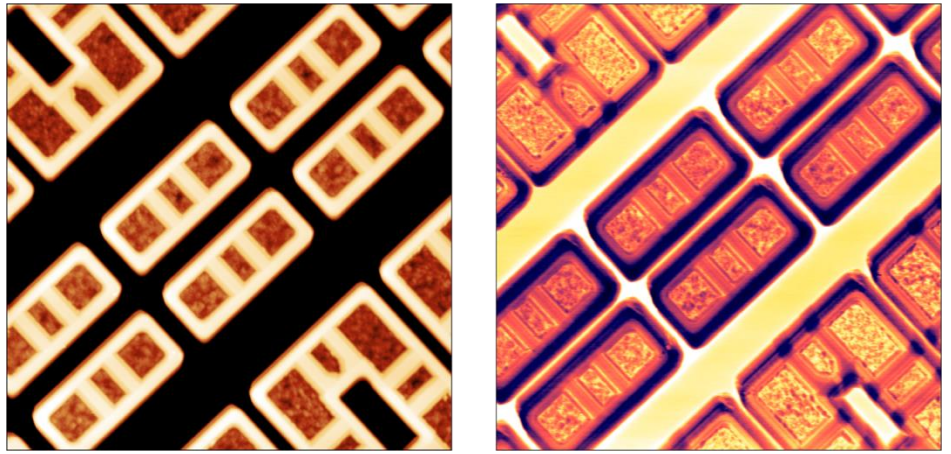




An S11 measurement (amplitude and phase) of a SCM sample, demonstrating high contrast between the areas of different doping levels

Proposed vs. Prior Art:

Parameter	Current Status	Proposed
Inspection of interconnects	Conventional AFM or STM can't detect interconnects buried under oxide layers. X-Ray and Electron Microscopy damage the oxide layer.	Scanning microwave microscopy (SMM) mode of AFM can non-destructively detect the interconnects with nanometer spatial resolution.
Electrical, Dielectric constant and Doping Density		Conductive and Scanning microwave microscopy (SMM) mode of AFM can non-destructively map electrical, dielectric properties and doping density with nanometer spatial resolution.



Topography (left) and capacitance (right) of a SRAM sample

Ref: https://www.nanosurf.com/en/scanning-microwave-microscopy

Skilling the Workforce in Local Engineering Colleges

Two-Tier Training Program

Online Coursework

- 100 engineering students from engineering colleges across Gujarat Students will be chosen at the end of their first year based on their interest and academic merit to participate in specialized online courses in Semiconductor Engineering domain offered by IITGN.
- These courses will be conducted online, allowing students to learn without leaving their home institutions or interrupting their studies. The curriculum will cover both foundational and advanced semiconductor manufacturing topics
- Credits earned from these online courses will contribute to the students' graduation requirements at their respective colleges or universities.

In-Person Practical Training

- At the end of their third year, around 50 students from the online program will be invited to IIT Gandhinagar based on their academic performance and aptitude for advanced lab work.
- These selected students will spend their final year at IIT Gandhinagar, focusing on practical, hands-on laboratory training to develop industry-relevant skills.
- 16 weeks of Industry Internship