Integrated Package Design

National Industry Co-Development Center (ICC) with Industry Consortium for Next Gen Research and Workforce

Rohit Sharma, IIT Ropar (Lead),

Sourajeet Roy, IIT Roorkee (Co-lead)

Dr. Jairam Sukumar, Qualcomm (Industry lead)

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Understanding the performance bottleneck

Current Density and Cross-sectional area Projection

Year	Maximum Tolerable Current Density	Maximum Current Density	Required Current Density	Cross-sectional Area

Current Density(MA/cm^2): 0, 2, 4, 6, 8, 10, 12, 14, 16, 18
Area(nm^2): 0, 200, 400, 600, 800, 1000, 1200, 1400, 1600, 1800
Year: 2014, 2016, 2018, 2020, 2022, 2024, 2026, 2028, 2030

Era of co-design

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International Technology Roadmap for Semiconductors, 2015. [Online]. Available: http://www.itrs2.net/itrs-reports.html

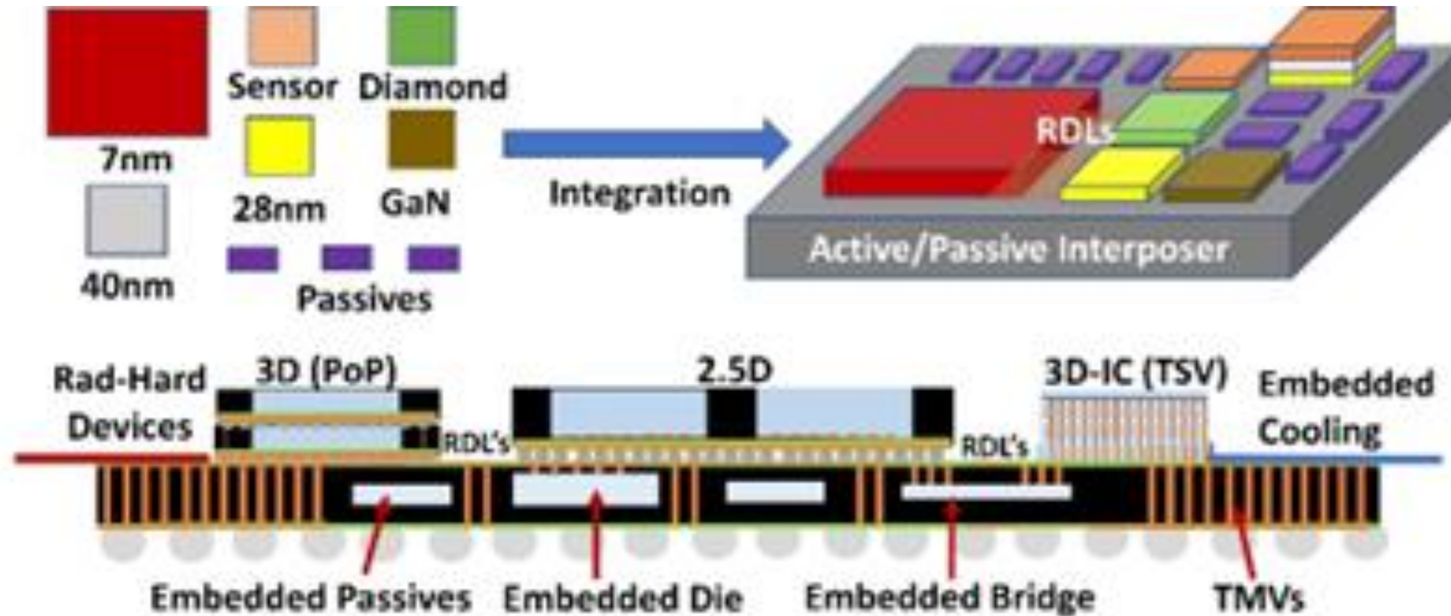
Integrated package design framework

Design

Materials

Processes

Environments



Electrical

Thermal

Mechanical

Reliability

Device Packaging	Bonding	Interposers	Interconnects
Wafer Level Packaging	Flip Chip	Organics	C4, Microbump's, Cu-Pillar
3D PoP, 3D-IC (Die Stack)	Thermo-Compression	Silicon	RDL's, TxVs, Optical
SiP, QFN, BGA, Hybrids...	Hybrid Direct Bonding	Ceramics	Cu-Cu (bumpless)

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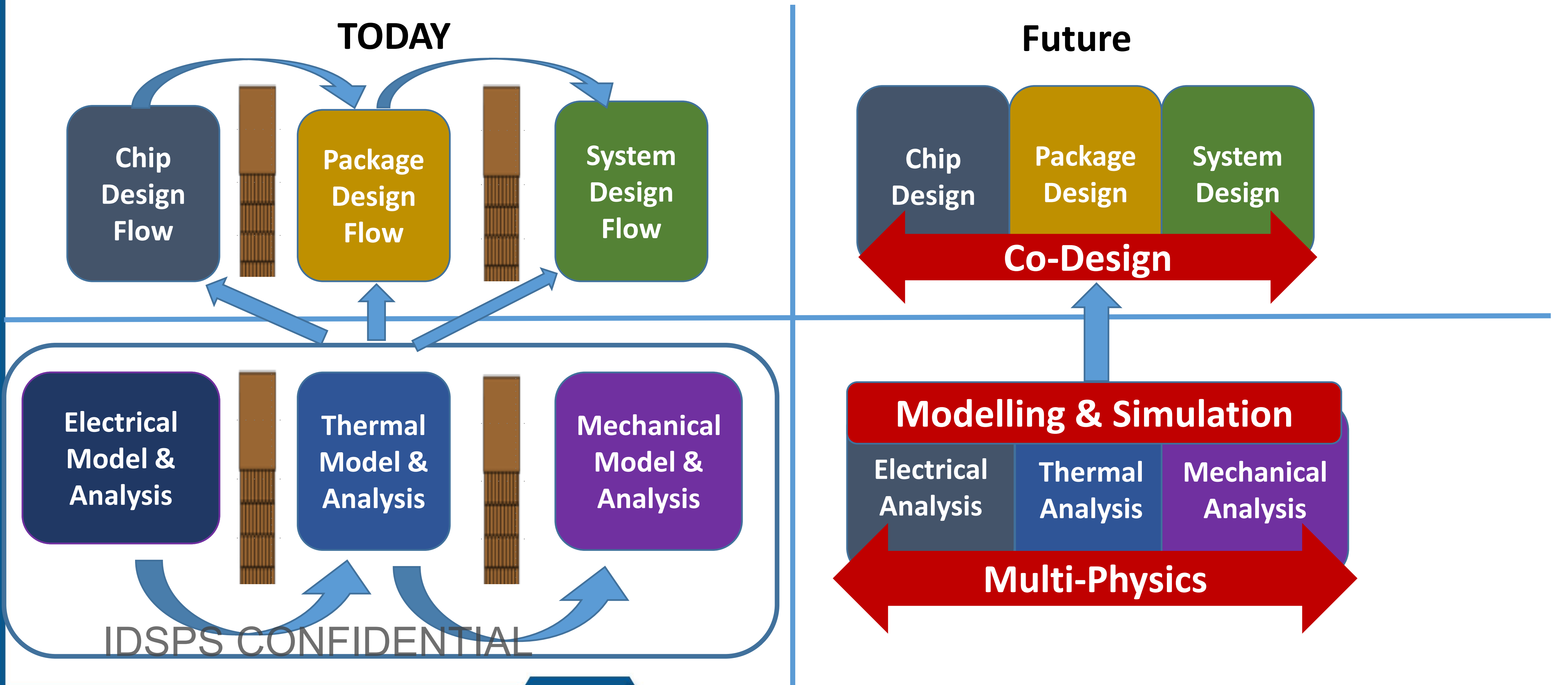

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Integrated package design framework

- **State of the art**
  - EDA Tools
  - High Fidelity Models: FEA, CFD, FDTD
  - Lower Fidelity Models: Compact models…
  - Point analysis tools
- **Several Challenges**
  - Electrical – SI/PI die-die coupling, parasitics
  - Thermal & Mechanical – Hot spots, Warpage
  - Multi-physics – Mobility shifts, Migration
  - System-Level models – AI/ML
  - Reliability – Physics of Failure
  - Materials – Stochastic behavior
  - Workforce

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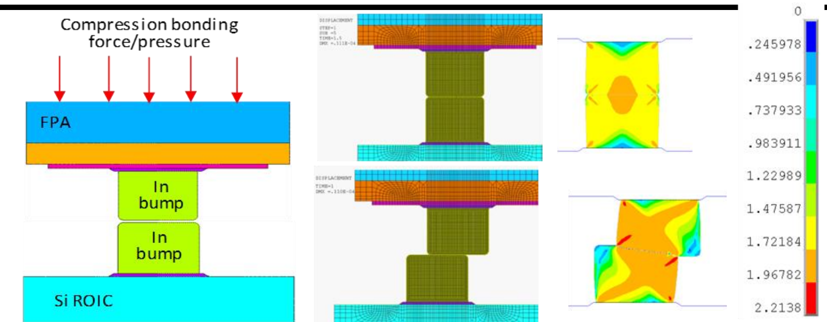

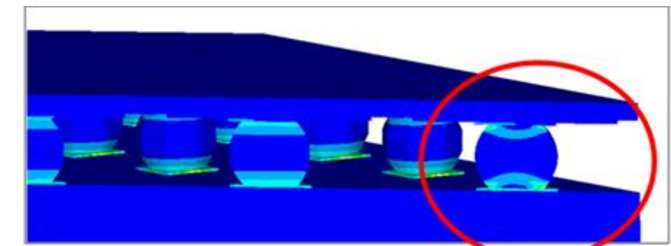

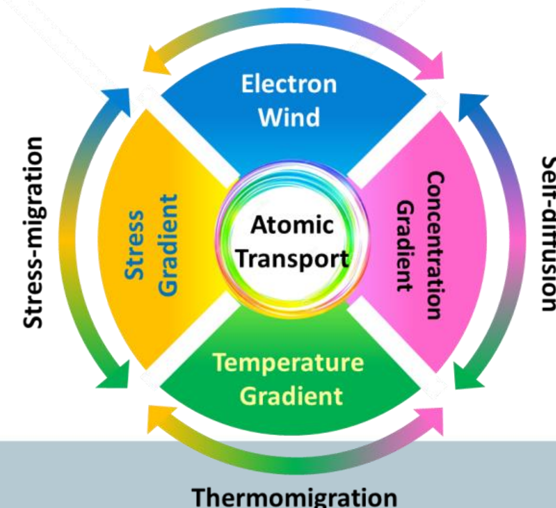

Integrated package design framework

Scale: Devices (nm) | Packages(um-mm) | Boards (mm-cm) | Systems (cm-m)

Data:
Materials
Manufacturing
Characterization;
Mission Profiles,
etc

Electrical & Optical
- Signal/Power Integrity
- EMI/Crosstalk
- Parasitics/Signal delays
- Optical attenuation
- Power Maps

Electro-thermal interactions

Electro-mechanical/chemical interactions

Design for Manufacture, Performance, Reliability & Robustness

Thermal
- Joule Heating
- Passive/Active cooling
- Hot spots
- Thermal resistance
- Thermal runaway

Thermo-mechanical interactions

Mechanical
- Stresses
- Fatigue
- Warpage
- Metal-migration
- Corrosion

Knowledge Base:
Design Rules,
PDK's ADK's, etc

Model Fidelity: Analytical | Circuit/Network | Compact/Response Surface | MOR | MD/FEA/CFD

Model based Optimization; Big Data Analytics; Physics of Failure Models; Prognostics; etc.

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Research Vision: Strategic focus areas and satellite centers

Project 1: Machine Learning Assisted Design Optimization of on-Chip Interconnects in Advanced Sub-10 nm Technology Nodes, **Sourajeet Roy, IIT Roorkee**
Project 2: Variability–Aware Modeling and Assessment of Jitter, **Jai Narayan Tripathi, IIT Jodhpur**
Project 3: Development of Multi-scale Predictive Electrothermal Model for reliability analysis of next gen package substrates, **Manodipan Sahoo, IIT Dhanbad**
Project 4: Electrical Characterization of Interfacial Crack Induced Reliability Issues in Redistribution Layer for 3D Heterogeneous Integration, **Manoj K Majumdar, IIIT Naya Raipur**
Project 5: Development of Packaging Technology for MMIC's & Semicon Chips, **Satinder K Sharma, Ranbir Singh and Robin Khosla, IIT Mandi**
Project 6: Performance Assessment of Interconnects in RF Packages at high frequencies and NN based performance optimization, **Yash Agrawal, DAIICT**
Project 7: Electrical, Thermal and Mechanical Analyses of TSVs using Machine Learning based Optimization Techniques, **M. Girish Kumar, VIT-AP University**
Project 8: Electrical-Thermal Co-Design for Next Generation Interconnect Pathways, **Rohit Sharma, IIT Ropar**

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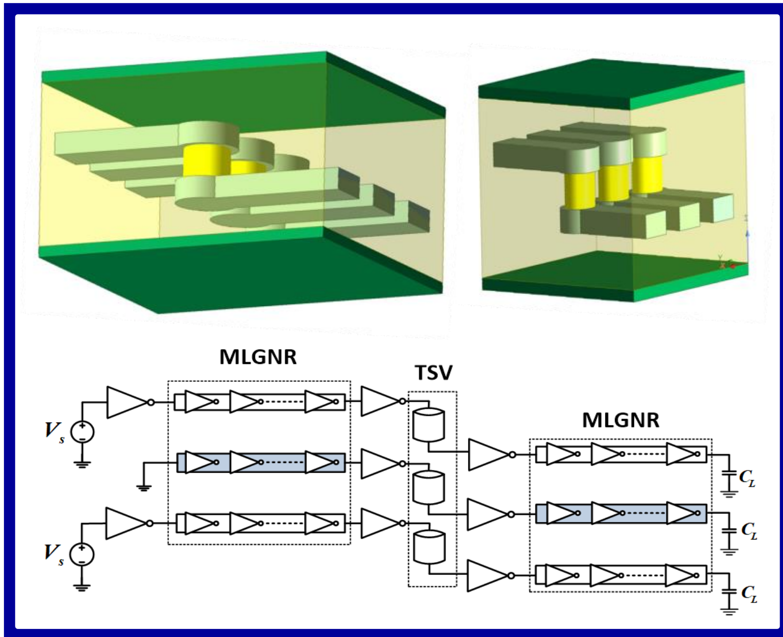
Project 1: Machine Learning Assisted Design Optimization of on-Chip Interconnects in Advanced Sub-10 nm Technology Nodes

PI : Sourajeet Roy (IIT Roorkee)

Objective: This project proposes to develop machine learning models of complex interconnects and via structures for extremely fast design optimization in sub-10 nm technology nodes



Technical challenges:

- In sub-10 nm, heterogeneous interconenects (e.g., Cu-graphene) are anticipated. However, these interconnects are very sensitive to fabrication process variations.
- Repeater optimization of such interconnects needs thousands of repeated SPICE simulations – too slow
- Traditional repeater optimization approaches usually under/overestimate the # repeaters

Outcome:

- Machine learning surrogate models of SI cost functions will be developed and parlyed as analytic models for extremely fast design space exploration. We anticipate design optimization times will shrink by one order of magnitude.
- We will consider device parameters (e.g., channel length, fin geometry, doping) as additional design parameters to achieve better optimal design.
- As bonus benefit, the optimized designs will need smaller on-chip real estate for repeaters (initial studie show 30-40% reduction in area)

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Project 2: Variability–Aware Modeling and Assessment of Jitter

PI : Jai Narayan Tripathi (IIT Jodhpur)

Objective: This project targets to investigate the faster assessment of impact of variability on timing budgets in high-speed circuits and systems

Technical challenges:

- Variability has become one of the major challenges as the scale of miniaturization is very high these days.
- Traditional methods like Monte Carlo (MC) simulations are not sufficient to get timely assessment of variability in modern high-speed circuits/systems.

Outcomes:

- To investigate the impact of variability on overall timing budget in a more comprehensive manner.
- To develop faster algorithms to assess variability.
- To contribute to industry standards e.g. IBIS.

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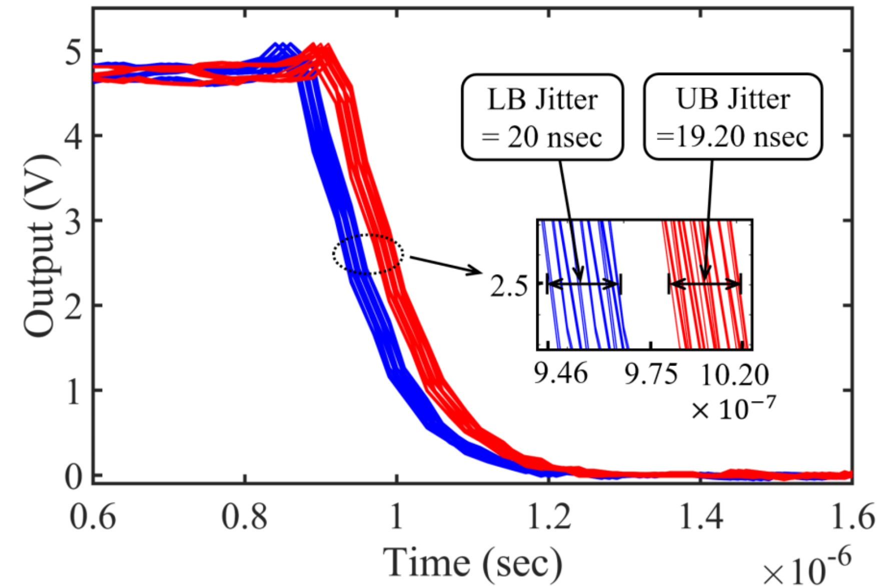


Fig: Measurement results of upper and lower bound jitter of the outputs due to power supply noise in two extreme samples of ICs.

References:

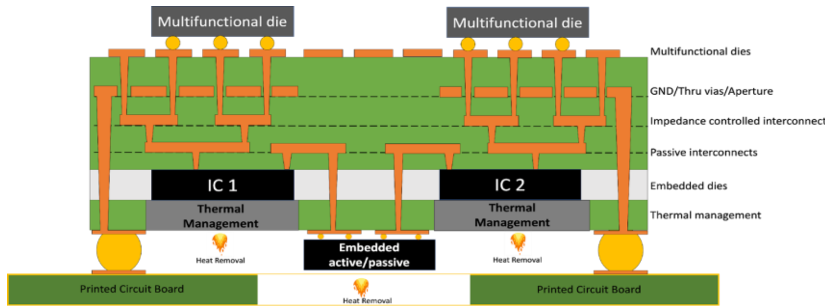
[1] V. K. Verma and J. N. Tripathi, “Variability-Aware Modeling of Power Supply Induced Jitter”, *IEEE Transactions on Signal and Power Integrity*, vol. 3, pp. 47-55, Feb. 2024.

[2] A. Chordia and J. N. Tripathi, "An Automated Framework for Variability Analysis for Integrated Circuits using Metaheuristics", *IEEE Transactions on Signal and Power Integrity*, vol. 1, 104-111, Sept. 2022.

Project 3: Development of Multi-scale Predictive Electrothermal Model for reliability analysis of next gen package substrates

PI : Manodipan Sahoo (IIT(ISM), Dhanbad) and Rohit Sharma (IIT Ropar)

Objective: To develop multi-scale, multi-physics based predictive Electrothermal Model for Next-generation package substrates.



Die embedded advanced packaging with fine pitch interconnect pathways

Outcomes:

- We propose to develop computationally efficient Multi-physics based compact electrothermal model for next gen packaged ICs to predict junction temperature and hotspots at chip, package and board levels based on the EMT (effective media theory) model.
- Electrothermal effects at nanoscale alongwith thermo-mechanical stress effects would also be included for precise estimation of reliability across chip, package and board levels.
- Machine learning-based surrogate model would be developed for real time prediction of failures across chip, package and board levels.

Technical challenges:

- Stacking more dies with each having high-density, fine-pitch *Cu* interconnects suffer from several coupled electrical, thermal, mechanical and chemical effects at different length and time scales leading to reliability issues.
- Particularly, High-voltage and mobile applications require accurate predictive electrothermal model for reliability estimation and analysis of the next-gen packages.
- Lack of robust Multi-physics based Multi-scale electrothermal Model for the advanced package substrates.

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	Prior art	**Proposed**
Compact Multiscale model	Non-compact models available	Compact multiscale model
Nanoscale thermal effects	Not included in Multi-physics	To be accounted for in Multi-physics
ML-based surrogate model	Not available	ML-based surrogate model

C. Wang et al., *IEEE Trans. VLSI*, vol. 32, no. 1, pp. 178-189, Jan. 2024

Project 4: Electrical Characterization of Interfacial Crack Induced Reliability Issues in Redistribution Layer for 3D Heterogeneous Integration

PI : Manoj K Majumder (IIIT Naya Raipur)

Objective: To investigate the effects of interfacial cracks on the performance and reliability of redistribution layer (RDL) structures in semiconductor packaging, particularly in high-density 3D Heterogeneous Structures

Figure -1: Influence of Interfacial crack in RDL layer of 3D IC

**RDL – Redistribution layer; W_{RDL}- Width of RDL; TSV – Through Silicon Via*

Technical challenges:

- The ultimate challenge is the reliability of ICs under real-world conditions, where defects such as interfacial cracks in the RDL can lead to performance degradation and increased vulnerability.
- In advanced semiconductor packaging, optimizing the manufacturing yield while maintaining high product quality is a continual challenge

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Outcome:

- The proposed RLGC model accurately estimate the influence of RDL defects, particularly interfacial cracks, with varying crack widths (0.18µm to 6.5µm) for the better estimation of via.
- It highlighted the significant difference in power loss during heating and cooling conditions, emphasizing the importance of temperature management. In addition, the low stress value suggests that the RDL can withstand substantial mechanical loads.
- The analysis address the challenges in fabricating RDLs, for better signal integrity, contributing to more efficient and reliable circuit designs.

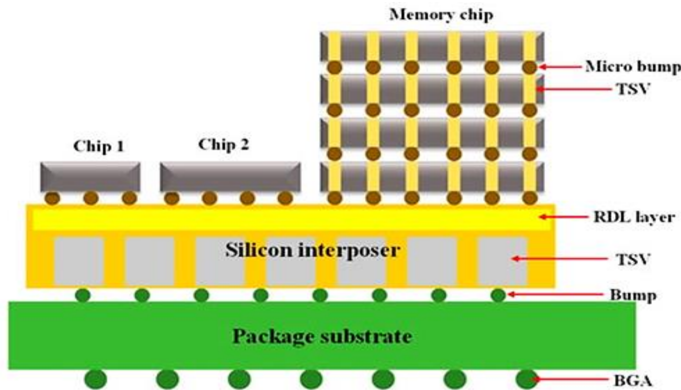
Parameters	Prior art	Proposed
Crack width	2.5 to 6.5 µm	0.18 to 6.5 µm
Stress	73.2 GPa	8.1 GPa
Insertion Loss in Heating	NA	-12dB
Insertion Loss in Cooling	NA	-6dB
Thermal Defect analysis in RDL	No	Yes

- S. Zhou *et al.*, “Stress Analysis of Typical Structure of Redistribution Layer of Fan-Out Wafer Level Package,” *2022 23rd International Conference on Electronic Packaging Technology (ICEPT)*, Dalian, China, 2022, pp. 1-5
- S. McCann, Y. Sato, V. Sundaram, R. R. Tummala and S. K. Sitaraman, "Prevention of Cracking from RDL Stress and Dicing Defects in Glass Substrates," in *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 1, pp. 43-49, March 2016.

Project 5: Development of Packaging Technology for MMIC's & Semicon Chips

PI : Satinder K Sharma, Ranbir Singh and Robin Khosla (IIT Mandi)

Objective: Our focus on optimizing fabrication processes, especially for GaAs and GaN technologies, positions us to push the boundaries of semiconductor nodes, ranging from 0.5μm to an impressive 0.15μm and beyond.



System-in-Package (SiP) Configuration

Outcomes:

- Implementation of power devices technologies will enhance MMIC capabilities, achieving power outputs up to 100W and operational frequencies ranging from 1 GHz to 100 GHz.
- Development of robust QFN and SiP packaging techniques to support enhanced thermal management and power efficiency.
- Establishment of scalable and efficient fabrication processes aimed at boosting manufacturability and yield, particularly for commercial and defense applications.

Technical challenges:

- **Integration Precision:** Precise control over power devices GaAs, GaN and analogous material properties is essential for high-frequency and power-efficient MMIC's and semicon chip packages.

- **Consistent Performance:** Ensuring uniform performance across 0.5μm to 0.15μm and beyond process nodes for QFN and SiP packaging, addressing thermal and power management challenges.

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Performance Metrics	Specification
Frequency Range	1 GHz – 100 GHz
Power Output (GaN-based PAs)	Up to 100W
Noise Figure (for LNAs)	<1 dB
Efficiency (Power Amplifiers)	>50%
Power Amplifiers Range	10W to 600W
Thermal Dissipation	Enhanced in QFN and SiP designs

Project 6: Performance Assessment of Interconnects in RF Packages at high frequencies and NN based performance optimization

PI: Yash Agrawal (DA-IICT Gandhinagar), Co-PI: Mekala Girish Kumar (VIT-AP)

Objective: This project aims to design, model, performance assessment and improvement of interconnects in RF packages and its optimization using neural network based approach.

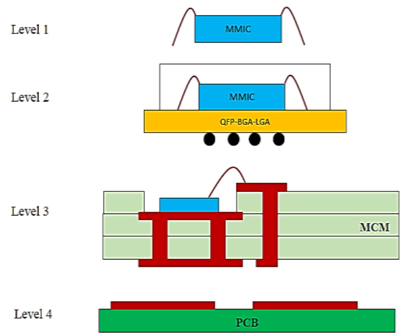

Fig. 1. RF packages and interconnections.

Technical challenges:

- At High fequencies (in the range of 10s to 100s of GHz, the signal integrity issues in interconnects detoriate significantly. The associated interconnect *RLC* parasitics cause various non-ideal effects.
- Also the die performance with interconnects in the RF packages at high frequency varies substantially due to loading, impedance mismatch issue, etc.
- Performance prediction and optimization is challenge and need to be addressed.

Outcome:

- Performance Assessment at high frequency levels Incorporation of performance improvement techniques such as current-mode signalling, emerging next-generation materials, circuit design methodologies for interconnections in RF packages.
- Formulation of electrical and analytical models
- Development of NN based models for performance optimization, signal integrity and variability analyses

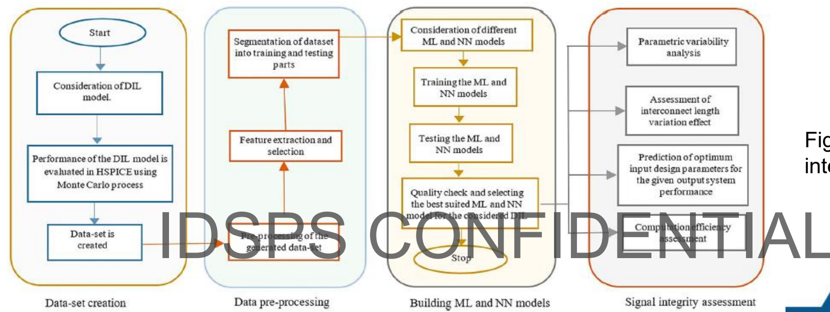

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Fig. 2. NN based model for interconnections

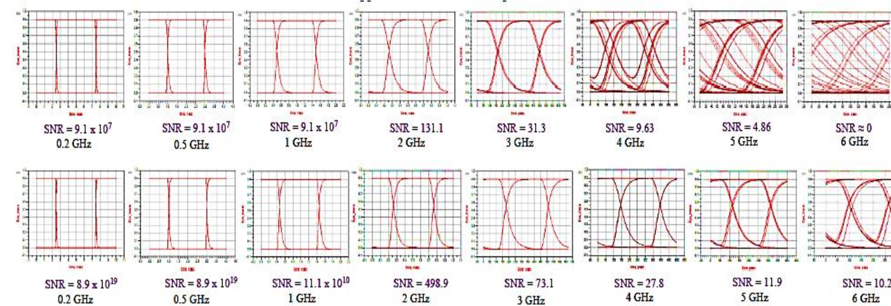


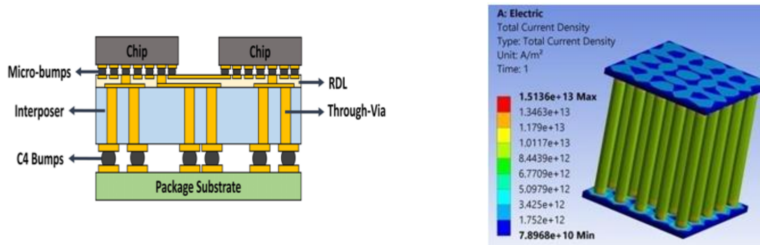
Fig. 3. Copper long Interconnections

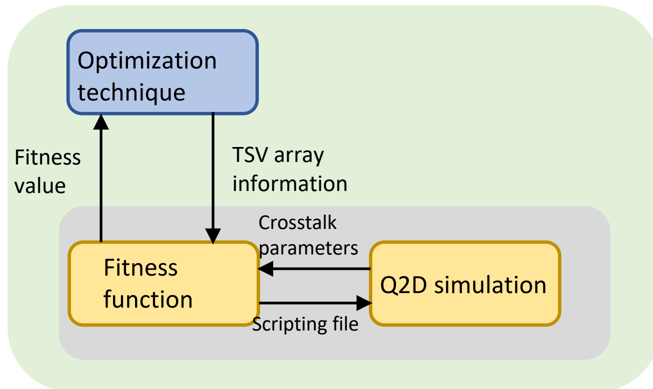
Fig. 4. Graphene long Interconnections

Project 7: Electrical, Thermal and Mechanical Analyses of TSVs using Machine Learning based Optimization Techniques

PI: M. Girish Kumar (VIT-AP University), Co-PI: Yash Agrawal (DA-IICT)

Objective: This project targets the electrical, thermal and mechincal analyses of TSVs using machine learning based huersitic approach optimization techniques





Co-simulation scheme of TSV array model

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Technical challenges:

- TSVs are used to transmit signals in high density array configuration, and they often face significant crosstalk challenges.
- In recent years, various methods have been explored to reduce the crosstalk such as guard ring, introducing the ABF material to increase the isolation layer, a ring of heavily doped p+ layer etc. However, these techniques would increase the manufacturing cost.

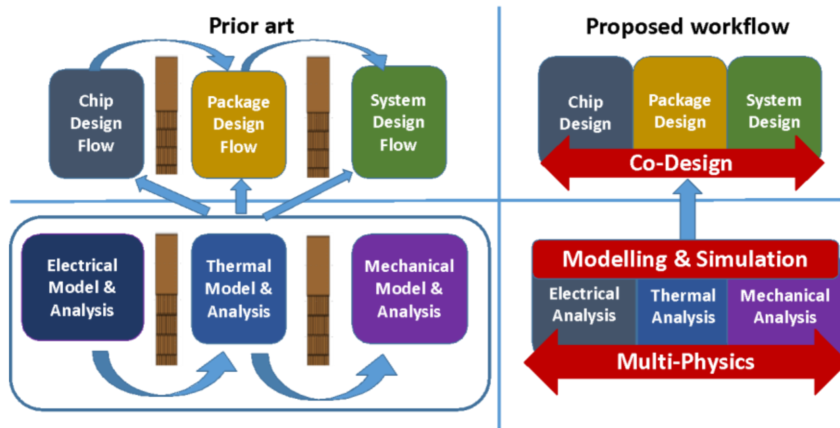
Outcomes:

- We propose a novel approach to conduct an ML based optimization technique for distribution of unfixed signal to ground ratio of TSV array.
- This approach is manily based on mechanical, themral and electrical performance evaluations.
- Investing the impact of through via gemoetry i.e. pitch and aspect ratio and array topologies i.e. square ana hexagonal.
- Providing the tradeoffs between the optimized design outcomes based on different optimization preferences.

Project 8: Electrical-Thermal Co-Design for Next Generation Interconnect Pathways

PI: Rohit Sharma (IIT Ropar)

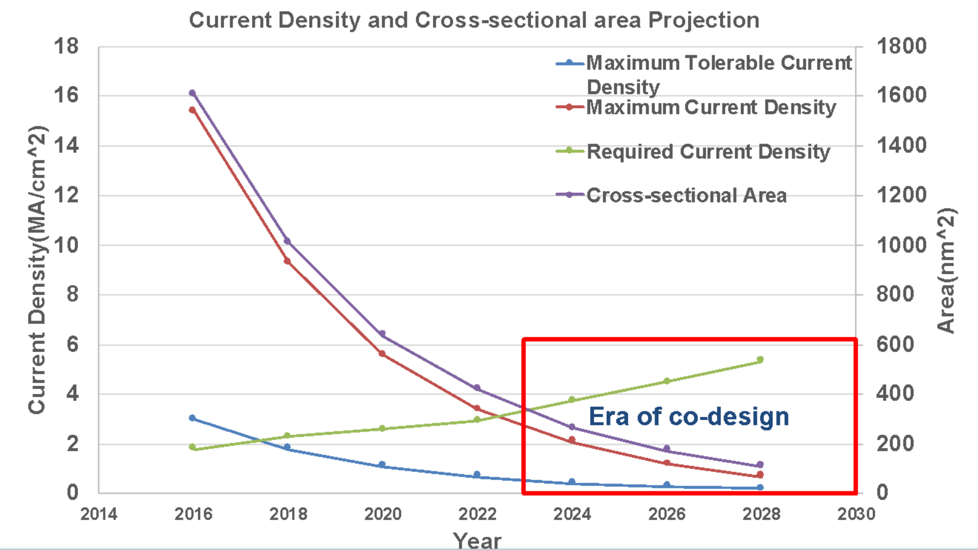
Objective: This project aims to develop a co-design methodology for high-performance interconnect pathways for chiplets-based near-memory compute engines in 3D packages



Proposed co-design workflow

Outcomes:

- Develop a comprehensive framework for electrical-thermal co-design in a heterogeneously integrated near-memory compute engine
- Improved *SI* and *TI* for hybrid interconnects considering process variations, discontinuities and material constraints for 3D packages
- Performance benchmarking of ultra-high-density hybrid interconnects against current *Cu* technology.



[Ref] Jeff Burns, "Systems and Architectures for Distributed Compute", *SRC Workshop*, 2022.

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List of Potential Industry Partners

- Qualcomm
- Intel
- Ansys
- Keysight
- Micron
- Global Foundries
- Kaynes
- Synopsys
- Cadence
- SCL Mohali

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Technology workforce development

- Current Courses at IIT Ropar:
  - Electronic Packaging
- New planned Courses:
  - Fundamentals of Signal and Power Integrity
  - Advanced Simulation Lab

	5 Years	10 Years
B.Tech	150+	500
M.Tech	100+	200
Ph.D	10+	30
Outreach	500	1500

- Planned Lab Courses for UG/PG students:
  - Hands-on training on the advanced simulation
  - Masters and PhD students working on industry-relevant challenges
  - Online courses/workshops for working professionals and technicians
    - 1-2 weeks certificate courses
  - Technicians' training of use of equipment
    - Month-long hands-on training of students at US collaborating institutions through short-term govt.- sponsored student exchange mobility grants
    - Global annual Ph.D. virtual summer school on Electronic Packaging

Target: 1500+ working professionals/ Technicians in the SI/PI domain through short-term seminars and certification in the next year 5 years

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5 Years Milestone Plan

Deliverable	Year 1		Year 2		Year 3		Year 4		Year 5	
Proposal Formation of SRA consortium with industry members	■	■								
Equipment procurement and installation	■	■	■							
Hands-on advanced design laboratory	■	■	■							
Definition of projects	■	■	■							
Set up primary research center		■	■	■						
Technology Demonstration and Development			■	■	■	■	■	■		
Design and demonstration prototype – 1				■	■	■	■	■	■	■
Design and demonstration prototype – 2				■	■	■	■	■	■	■
Educate Graduate students PhD : 10+, MTech: 30+ within Institute			■	■	■	■	■	■	■	■
Train 2000 students, researchers, engineers and technicians through the educational outreach programmes			■	■	■	■	■	■	■	■

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5 Years Budget for NIC and satellite centers

- Equipment: INR 15 cr
  - Servers, workstations
- EDA tools: INR 20 cr
  - EM, Circuit simulation, SI/PI simulation, Thermal
- Manpower: INR 10 cr
  - Grad students, research faculty, project staff, admin staff etc.
- Travel and contingencies: INR 1.5 cr
- Overheads: As applicable
- **Total: INR 55 cr**

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Thank you

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