इंडिया सेमीकंडक्टर मिशन

India Semiconductor Mission

Catalyzing India's Semiconductor Ecosystem

Projects
and
Plans

Industry Co-development Center (ICC)

on

Next Gen System Level Electrical Test

Faculty Lead: Jaynarayan T Tudu, IIT Tirupati
Faculty Co-Lead: Satyadev Ahlawat, IIT Jammu

Industry lead: Navin Bishnoi, Marvell
Industry Co-lead: Paresh Bharkhada, Teradyne

Industry Needs and Challenges [HIR 2024]

Fig:
Test H/W cost per IC unit shipped. ATE dominates

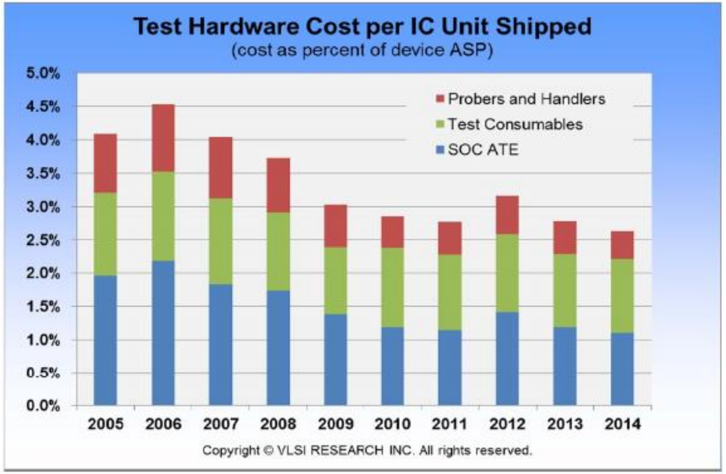


Fig:
Test cost distribution
In pie chart

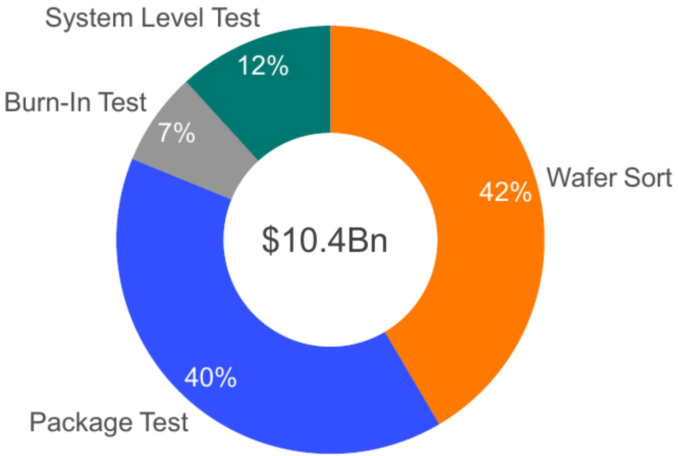


Fig:
Test Market cost is increasing
In $Bn

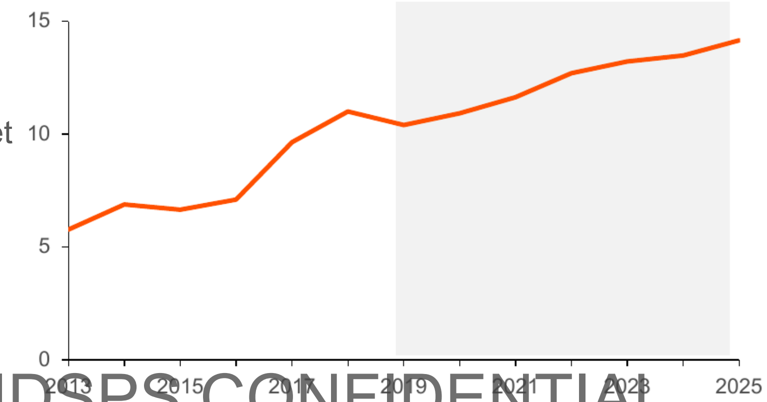
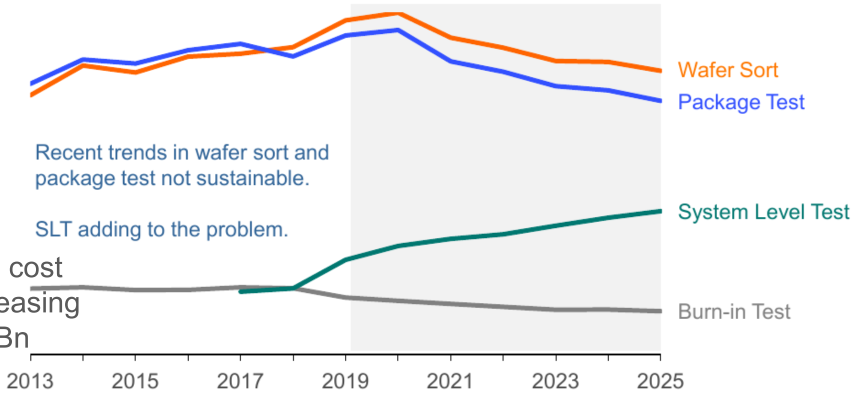
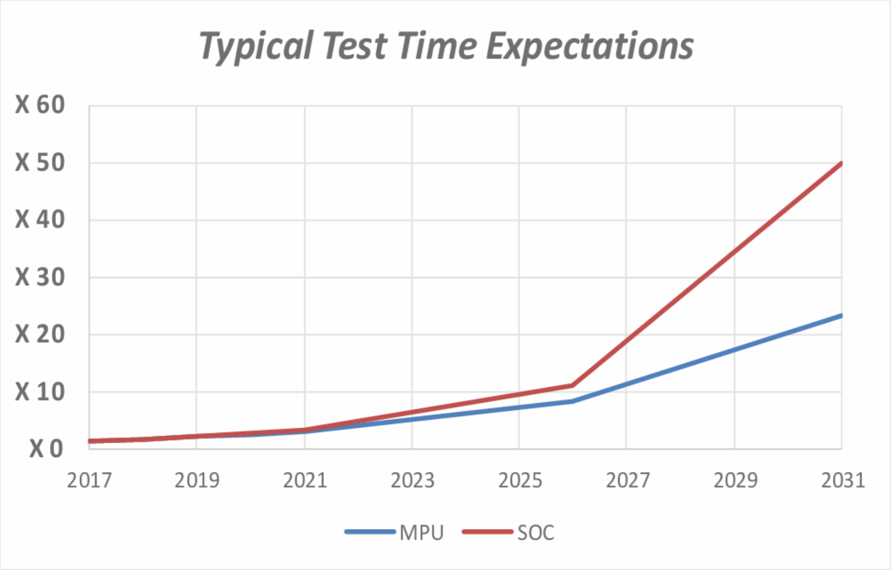


Fig:
SLT cost increasing
in $Bn



Industry Needs and Challenges [HIR 2024]



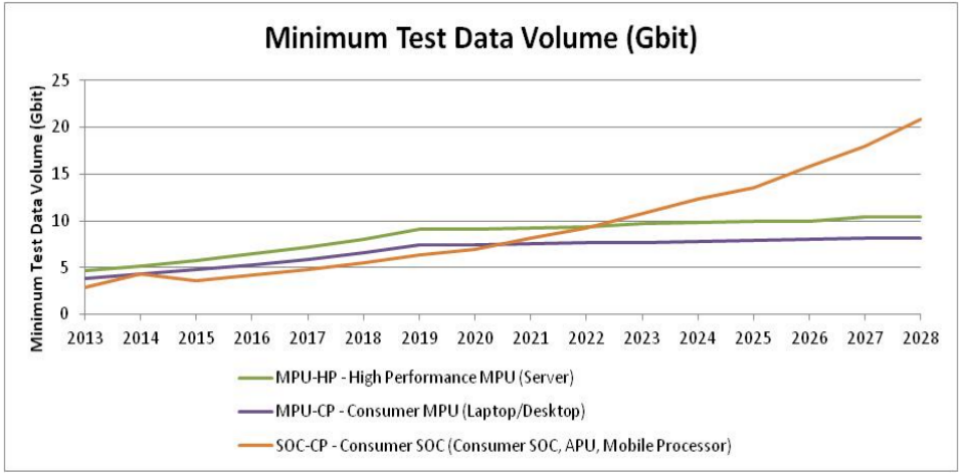


Fig: Test Time will increase In SoC and MPU

Fig: Test Date Volume will increase In SoC and MPU

Reference: Heterogenous Integrated Roadmap, 2024

Industry Needs and Challenges [SLET Team]

1. Chiplet test: Testing **interconnects** (atpg algorithm) and the newer faults- resistive **short and open** is challenging, chiplet test **standard**.
2. System level test: Structural test escapes, marginal defects, no appropriate **fault model**, complex hardware/**software** system, advanced node, and complex process.
3. Yield improvement:Trading-off with the test quality, test cost, and test power.
4. Test cost: Reducing test data volume, test time, and test power as complexity increases.
5. DFT turn around time: Design complexity, additional **SLT flow** posing challenges to turn around time
6. Silent data corruption: complexity of data center, **root-cause analysis**.
7. Silicon life-cycle management: addressing the **yield and process** issues.
8. Realtime data analytics: how to feed-back the test data for test test optimization and yield Improvement.
9. Efficiency improvement: reducing months to week of ATE time.
10. AMS testing: coverage matrix, fault model, and self testing.

Reference: The inputs received from the industrial experts of companies such as Qualcomm, Synopsys, Teradyne, Marvell, Western Digital, Siemens etc and from the academic researchers.

Where do We Stand Globally

OPEN Compute Project

SYSTEM IN PACKAGE TESTING

HIR

HETEROGENEOUS INTEGRATION ROADMAP

2024 Edition

Chapter 17: Test Technology

- These two global society also have parallel goal as SLET
- The area of our future interest

  Memory Test: HBM, ReRAM.

  Probe Device Handling: wafer level thermal issues.

  RF Test and Photonics Test.

Objective

Research:

- Next generation research problems
- R & D infrastructure
- 3D Chiplet technology development
- R & D reinforce to Industries

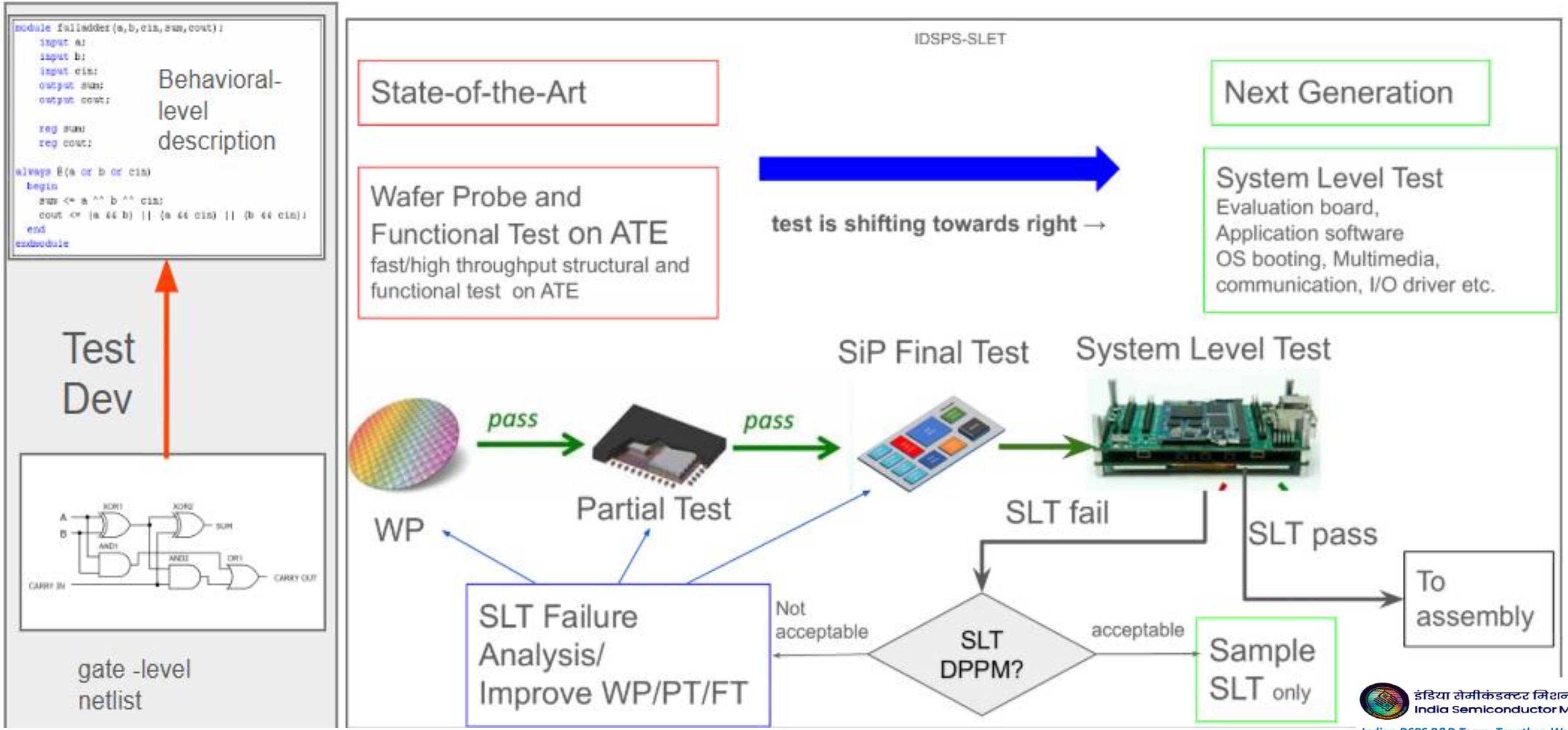
Education:

- Curriculum on next gen technology
- Educational infrastructure
- Educational program
- Workforce development

Industry:

- Industry consortia
- Technology transfer and commercialization
- Start-up creation
- Industry-Academia collaboration
- Training to industry engineers

Vision: Strategic Research Approach



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Indian DSPS R&D Team: Together, We Can.

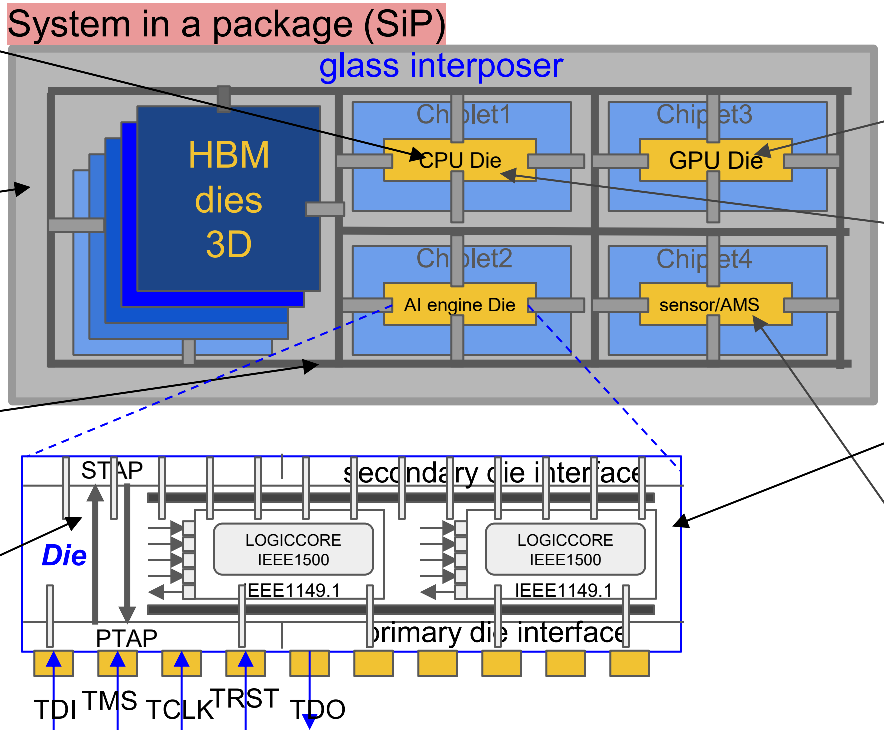
Vision: Strategic Research Areas

Diagnosis and Post Silicon Debugging
Institute: IIT Jodhpur [Binod]

Chiplet Test Architecture and SLT
Institute: IIT Tirupati [Jaynarayan]

System Level
Chiplet Interconnect Testing
Institute: IIT Tirupati [Vikramkumar]

Boundary Scan and Security
IIT Jammu [Satyadev]



PnR of Internal Scan Chain and
Low-power ATPG Algorithm
IIT Bombay [Virendra, Rohit]

Processor Functional Testing
Cochin Univerity (CUSAT) [Tripti]

KGD, DPPM and ATE Machine
Marvell India [Nikhil]

Analog and Mixed Signal Faultmodeling
Still open

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Indian DSPS R&D Team: Together, We Can.

India-wide Faculties and Expertise

Jaynarayan T Tudu (IIT Tirupati)
(Chiplet DFT, Accelerator test, SLT)
Primary ICC

Satyadev Ahlawat (IIT Jammu)
(Boundary scan, H/W Security)
Satellite ICC

Binod Kumar (IIT Jodhpur)
(Defect diagnosis and PSD)

Vikramkumar Pudi (IIT Tirupati)
(Chiplet interconnect testing)

Tripti S Warrier (CUSAT Cochin)
(Processor functional testing)

K D Patel (S P University)
(Burn-in Testing)

Virendra Singh IIT Bombay
(Internal Scan DFT,
Power-aware ATPG, CPS Testing)

Potential Faculties: Indranil Sengupta, IIT Kharagpur **(Test EDA, Memory),** Bhargab Bhattacharya, IIT Kgp **(DFT and ATPG),** Susmita Sur-Kolay, ISI Kolkata **(ATPG and Reliability)**, S Sivanantham, VIT Vellore **(ATPG and Security),** N N Murthy, IIT Tirupati **(Device Reliability), Ayan Palchaudhury, IITBBS (Testability).**

Cross SRA Faculty Experts: SDA, ICBAR, and 6GIS

Nandita Rao, IBM
[System Design and Architecture]

Binod Kumar (IITJ)
[System Design and Architecture]

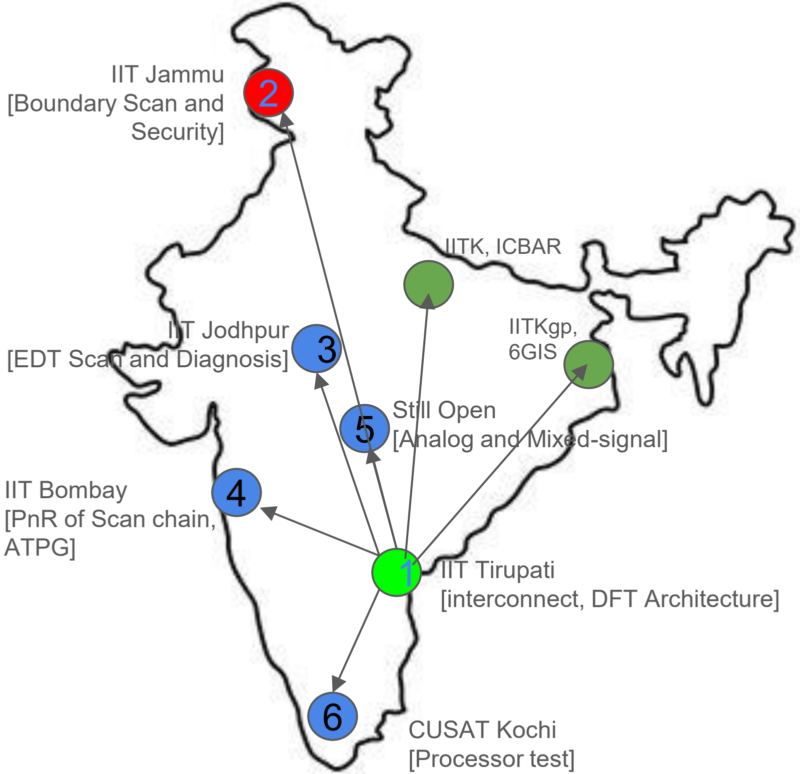
Nilesh Badwe (IITK)
[IC and Board Assembly and Reliability]

Mrinal Mandal
(IIT Kgp)
[6G Integrated System]

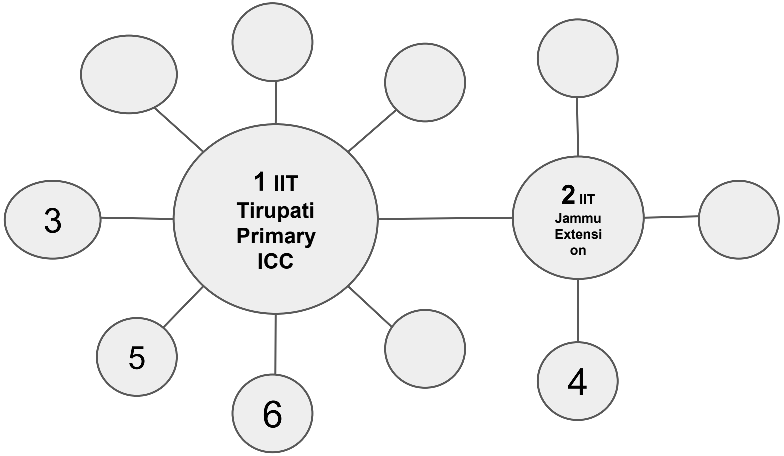
Siddhartha Duttagupta
IIT Bombay
[6G Integrated System]

ICC: Hub and Spoke Model

ICC and Research faculty



Hub and Spoke Model



- Cross SRAs
- Primary ICC
- Satellite ICC
- Research faculty

Global Partners and Industry Experts

Global Academic Collaborators

Abhijit Chatterjee,
Georgia Tech, US
[Analog and mixed-signal test]

Adit Singh, Auburn University, US
[System level test/ATE]

Industry Collaborators:

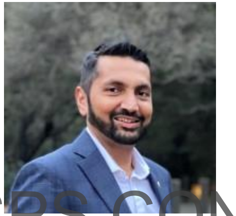
Navin Bishnoi, Marvell
[Low Power DFT]

Nikhil Sudhakaran, Marvell
[KGD, DPPM, ATE, Functional Test]

Kamlesh Pandey, Krivya Semicon
[EDA for Test, ATPG]

C P Ravikumar, Sykatia
[EDA for Test, ATPG]

Paresh Bharkhada, Teradyne
[ATE Machines]



Suraj Sindia, Intel USA
[AMS and Parametric Testing]

Potential collaborators:

Prakash Talwar, SanDisk, IN
Ankush Srivastava, Qualcomm, IN
Kuralla Vikram, AMD, IN
Sykatia Pvt Ltd, IN

Research Projects

1. Low-power Design-for-Test Architecture for Chiplet System in Package
   Lead: Jaynarayan T Tudu (IIT Tirupati)
1. Physical Design Aware ATPG Algorithm for Low-power Testing
   Lead: Virendra Singh (IIT Bombay), Rohit Badjatya (IIT Bombay)
1. Side-channel Attack Resilient Stream Scan Architecture
   Lead: Satyadev Ahlawat (IIT Jammu), Gaurav Kumar (IIT Jammu)
1. High-speed System-level Testing of 3D Chiplet Interconnect
   Lead: Vikramkumar Pudi (IIT Tirupati)
1. DPPM Reduction & System correlation through targeted Functional Tests on ATE
   Lead: Nikhil Sudhakaran (Marvell India), Navin Bishnoi (Marvell India)
1. Automated Software Based Test Generation Framework for Scalar RISC-V Processors
   Lead: Tripti S Warrier, CUSAT; Neel Gala, InCore Semiconductors
1. Multi-EDT Multi-Fault Scan Chain Diagnosis Methodology with Deep Learning
   Lead: Binod Kumar (IIT Jodhpur)
1. Extending Fault Modeling for Enhanced Test Coverage of High-speed AMS Circuits
   Lead: Suraj Sindia, Intel USA. We are looking for faculty collaborator.
1. Design and Fabrication of a Dual Mode Thermal Stress Burn-in Test System for Semiconductor Devices Using Indigenous Algorithms.
   Lead: K D Patel (Sardar Patel University, India)

Project 1: Low-power Design for Test Architecture for Chiplet System-in-Package

Team: Jaynarayan T Tudu, IIT Tirupati, Binod Kumar, IIT Jodhpur

Objective:

- To address the test power problem (average and peak) during scan shift and launch operations. The new architecture will be the improvement upon the existing streaming scan architecture.
- To carry out power analysis of the streaming scan architecture during shift and launch
- To extend the architecture to address the scan test power problem for 3D-chiplet based SiP design.

Project goal:

- Generate an IP on the new low-power streaming scan architecture.
- Incorporation of the proposed architecture into the existing test standard

Proposed vs prior-art:

	Current state [1, 5]	Proposed
Test time (in cycle)	2 to 3 million for 10K pattern	1 to 2 million (parallel)
Test data volume (in bits)	90 to 100 Mb for 10K pattern	Remain same (hard problem)
# I/O Pins	5 to 10 pins	3 to 5 pins (outer serialization)
Test clock (shift speed)	100 to 500 MHz	500 MHz (by power minimization)
Test power	___________	~1.5 to 2 times the functional power

Fig 1: Existing design- Streaming Scan architecture [1]

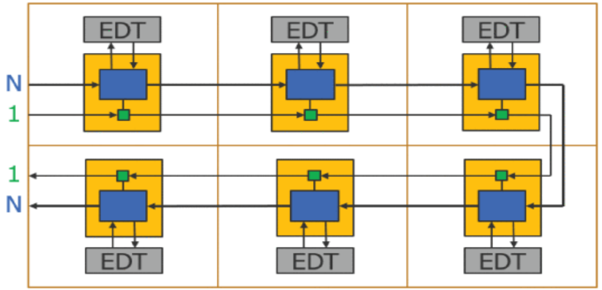
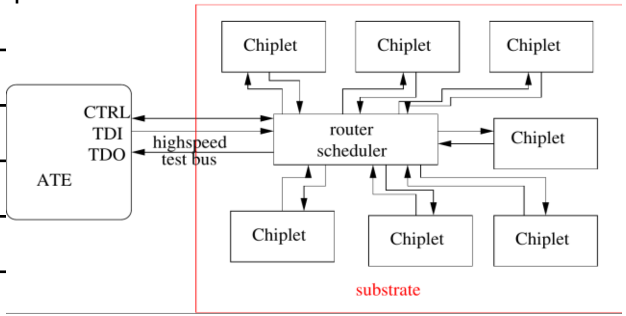


Fig 2: Proposed design: Low-power Hierarchical streaming scan



References:

1. Jean-François Côté, Mark Kassab, Wojciech Janiszewski, Ricardo Rodrigues, Reinhard Meier, Bartosz Kaczmarek, Peter Orlando, Geir Eide, Janusz Rajski, Glenn Colón-Bonet, Naveen Mysore, Ya Yin, Pankaj Pant, Streaming Scan Network (SSN): An Efficient Packetized Data Network for Testing of Complex SoCs. ITC 2020: 1-10

2. Erik Jan Marinissen, Teresa L. McLaurin, Hailong Jiao, IEEE Std P1838: DfT standard-under-development for 2.5D-, 3D-, and 5.5D-SICs. ETS 2016: 1-10

Project 2: Physical-design Aware ATPG Algorithm for Low-power Testing

Faculty Lead: Virendra Singh (IIT Bombay), Rohit Dajatya (IIT Bombay)

Objective:

- Investigation of the influence of physical design parameters on test power and failures
- Design and development of ATPG algorithm considering the physical design parameters
- Co-optimization of the ATPG algorithm and scan architecture given the physical design parameters as constraints.

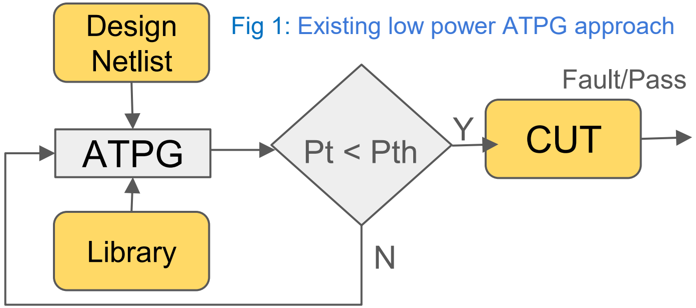


Fig 1: Existing low power ATPG approach

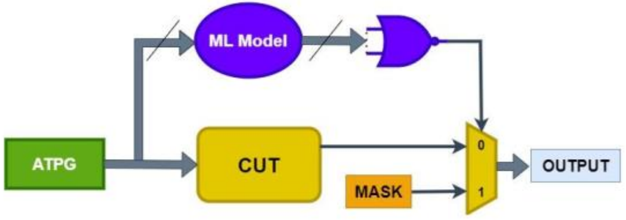
Project Goal:

- Hot-spot and IR droop free test methodology (test power problem needs to be solved)
- IP creation: Seamless integration of the new test methodology with the existing ones (plug-and-play solution approach)
- Efficient utilization of design parameters for design-for-test insertion and ATPG algorithm (learned design decision making)

Proposed Methodology and Architecture:

- Layout data collection
- Partitioning
- Ml Model Training
- Realtime hotspot detection
- Fault-tolerance response masking

Architecture:



	State-of-the-Art	Proposed
Vdd droop/Vss bounce	800 mV/62mV (1M gate)	850mV-900mV/20mV-40mV
# Hotspot areas	10 to 20% area [4]	0 to 5%
Peak power	10 to 15 time functional peak	<= functional peak
Average power	No more a problem	Exiting solution

Reference:

1. T. Utsunomiya, R. Hoshino, K. Miyase, S. -K. Lu, X. Wen and S. Kajihara, "Effective Switching Probability Calculation to Locate Hotspots in Logic Circuits," *2022 IEEE International Test Conference in Asia (ITC-Asia)*, Taipei, Taiwan, 2022, pp. 43-48,

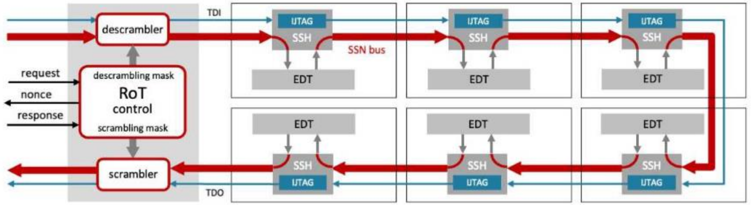
Project 3: Side-channel Attack Resilient Streaming Scan Architecture

Team: Lead: Satyadev Ahlawat, IIT Jammu; Gaurav Kumar, IIT Jammu; Anjum Riaz, IIT Jammu

Objective:

- To address the security issues in advanced scan architectures for chiplet based 2.5D and 3D chiplet based SiP
- The proposed security mechanism will be integrated into the existing streaming scan network (SSN)
- Test authorization and scan data encryption by leveraging IJTAG's SIB and using stream ciphers to fortify the existing SSN against scan attacks

Existing design: RoT SSN



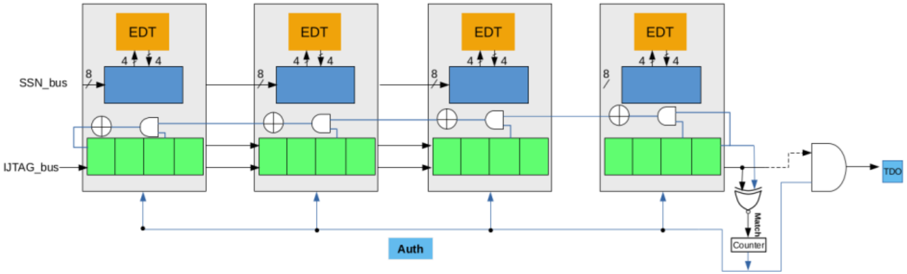
Project goal:

- Develop an IP on secure SSN
- Integration of the proposed architecture into the existing industrial DfT flow

Existing Vs Proposed:

Parameter	Existing	Proposed
DFT Area	High	Nominal
Scalability	Poor	High
Computational overhead	Secure server	No

Proposed design: ISSIB based SSN



1. J. Rajski, M. Trawka, J. Tyszer and B. Włodarczak, "Hardware Root of Trust for SSN-basedDFT Ecosystems," *2022 IEEE International Test Conference (ITC)*, Anaheim, CA, USA, 2022, pp. 479-483,

Project 4: High-speed System-level Testing of 3D/2.5D Chiplet Interconnect

PI - Vikramkumar Pudi, Co-PI: Jaynarayan T Tudu, IIT Tirupati

Objective:

- Examining the effectiveness of structural test for weak open and short defects.
- Modeling the interconnect open/short defect as path delay fault.
- Investigating on the system level fault model for interconnect defects
- Testing the signal integrity and degradation using delay test methodology
- Using the UCIe protocol to perform system level test

Project Goal:

- To develop a system level test for high-speed interconnect.
- Complying with the IEEE standard P3405
- IP generation towards SLT for interconnect testing

Existing Vs Proposed:

Parameters	State-of-the-art	Proposed
Structural Vs SLT	Structural (Short & open)	SLT-system level
High-speed	partially	Yes
Fault Coverage and Pattern count	Structural = ~97%, SLT = 0%	Structural = ~ 97% + SLT = 3%

Fig 1: Existing structural test method + extended to transition pattern [1]

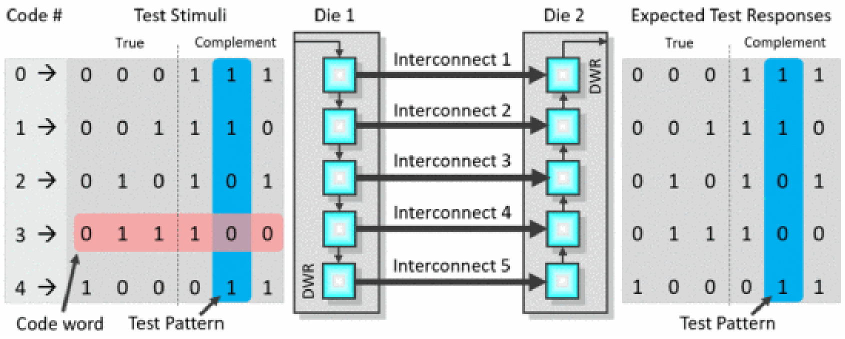
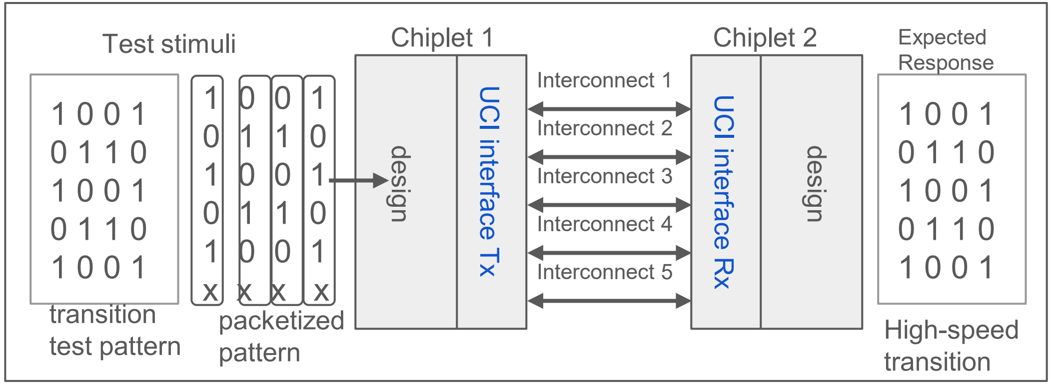


Fig 2: Proposed system level test with packetized pattern using UCIe protocol



Reference:

1. Y. Chuang *et al.*, "Effective and Efficient Test and Diagnosis Pattern Generation for Many Inter-Die Interconnects in Chiplet-Based Packages," *2023 IEEE International 3D Systems Integration Conference (3DIC)*, Cork, Ireland, 2023

2. Das Sharma, D., Pasdast, G., Tiagaraj, S. *et al.* High-performance, power-efficient three-dimensional system-in-package designs with universal chiplet interconnect express. *Nat Electron* 7, 244–254 (2024).

Project 5: DPPM Reduction & System correlation through targeted Functional Tests on ATE

Team: Lead: Nikhil Sudhakaran, Marvell, Navin Bisnoi, Marvell; Faculty Lead: Jaynarayan, IIT Tirupati

- **Problem Statement/Objective**
  - Manufacturing tests mostly depends on Structural/loopback testing on ATE and SLT for Functional/system level testing-
    - Separate platform needed because of the low correlation of ATE Structural tests w.r.t SLT
  - Define a generic and standardized Test Architecture & Methodology to drive targeted testing of all Functional blocks in Design on ATE.
  - Achieve higher coverage over and above standard Structural tests like Scan, MBIST, LBIST and reduce overall DPPM
  - Achieve Highest level of correlation between Manufacturing testing and System-level/Field level testing – Reduce SLT dependency
- **Project Goal**
  - Define architecture and a protocol – Design, verify IP and associated components to enables End to End functional test on ATE
  - Fault-Grade new functional vectors along with DFT tests (Scan/MBIST)
- **Proposed vs Prior Art.**

- **Existing Design**
  - Standard Structural Test-Structures(Scan,MBIST,BSCAN)
  - Analog/PHY IP-testing via JTAG (Loopbacks, Spot-Checks)
  - No targeted functional test architecture
- **Proposed Design(s)**
  - Functional Test-Infrastructure added on top of existing Structural/ tests
  - Approach 1
    - Standard (Serial/Parallel bus) Slow-speed interface to push in Functional test-code (test respective block) to internal memory
    - Boot-CPU picks up test-code and executes test internally
  - Approach 2
    - Protocol Aware BIST logic (FSM + logic) added which will trigger data-traffic through system protocols like AXI/AHB mimic exact system/E2E data traffic – Internally generate PASS/Fail
  - Additional approaches to be evaluated as part of research.

Test-Metric	Current State (Structural Tests only)	Proposed (Structural + Functional Tests)
DPPM	Higher- Only through Structural & Loopback coverage	Lower- Additional functional tests reduce DPM impact
ATE to System Correlation	Low (No direct correlation between Structural tests & System)	High (New Functional tests mimic System scenarios)
SLT Test-Time & Cost	Higher – Due to requirement of running all Functional tests.	Lower (~50%) – Fewer tests on Volume SLT
ATE-Test-Time & Cost	Marginally lower due to lesser test-content	Marginally higher (~5%) – As some func.tests are added
IO-Requirements	Baseline	Serial i/f – No change (Can use JTAG), Parallel i/f – Min to Zero (Sharing with GPIOs/Scan), Internal-BIST – No change (can use JTAG)
Area-Overhead	Baseline	~0.3-0.5% increase due to additional logic

Reference:

M. De Carvalho, P. Bernardi, E. Sanchez, M. S. Reorda and O. Ballan, "Increasing fault coverage during functional test in the operational phase," *2013 IEEE 19th International On-Line Testing Symposium (IOLTS)*, Chania, Greece, 2013,

Project 6: Automated Software Based Test Generation Framework for Scalar RISC-V Processors

Team: Lead: Tripti S Warrier, CUSAT; Neel Gala, InCore Semiconductors

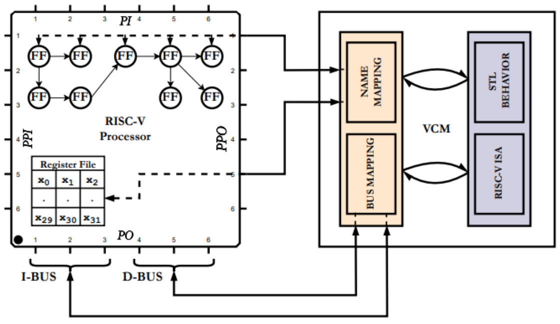
Objective:

- Generate a comprehensive test strategy for defect detection to guarantee reliability and quality of RISC-V cores without the overhead of Design for Testability (DFT) infrastructure .
- To automate generation of Software-Based Self-Test (SBST) programs for
  - at-speed & in-field testing to identify static faults in processor cores by running software programs.
  - functional testing of physical units of the core.

Project goal:

- Cost-effective software based test for Standard Test Libraries to test RISC-V cores.
- Tests for functional units inside the core that can achive coverage for various static faults too.
- To come up with a processor-agnostic approach of reusing constraints to handle all the RISC-V extensions.

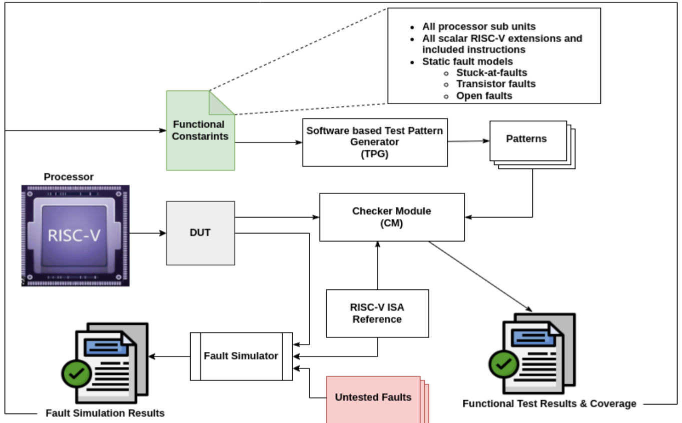
Existing design: Constraint based automatic SBST generation using BMC solvers



Proposed Vs State-of-the-art:

	Current [1]	Proposed
Defects addressed	Only stuck-at fault	All static faults & functionality testing
Physical units covered	ALU & Registers only	Entire functional units inside the core
Fault coverage	93%	95% - 99%
Methodology	BMC solver	Formal methods

Proposed design: configurable software based test generation for scalar processor



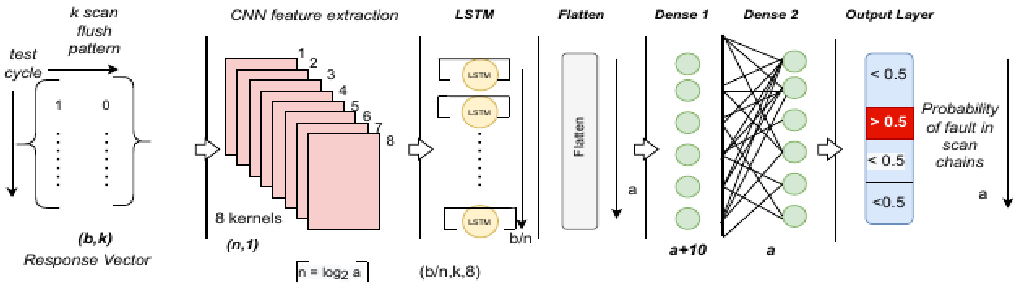
Reference:

1. T. Faller, N. I. Deligiannis, M. Schwörer, M. S. Reorda and B. Becker, "Constraint-Based Automatic SBST Generation for RISC-V Processor Families," *2023 IEEE European Test Symposium (ETS)*, Venezia, Italy, 2023, pp. 1-6, doi: 10.1109/ETS56758.2023.10174156.
2. A. Riefert, R. Cantoro, M. Sauer, M. Sonza Reorda and B. Becker, "A Flexible Framework for the Automatic Generation of SBST Programs," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 10, pp. 3055-3066, Oct. 2016, doi: 10.1109/TVLSI.2016.2538800.

Project 7: Multi-EDT Multi-Fault Scan Chain Diagnosis Methodology with Deep Learning

Binod Kumar (IIT Jodhpur)

Fig 1. The existing single EDT scan chain diagnosis model



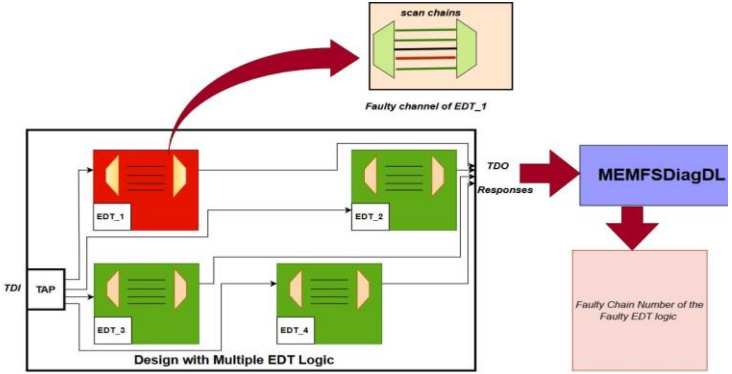
Objective:

- Development of methodology of scan chain diagnosis of multiple EDT structures utilized in chiplet-based next-gen architectures
- Alternative to one-hot test pattern generation from commercial tools.

Proposed work plan:

- We plan to develop highly accurate Deep Learning (DL)-based scan chain diagnosis methodology for multiple faults scenarios in manufacturing test (MEMFSDiagDL)
- No requirement of special diagnostic test pattern generation leading to quick turnaround time
- 2-step methodology is proposed: first identification of faulty EDT within a multi-EDT environment and second, the subsequent suspect scan cell identification
- Minimum aliasing is targeted to achieve high accuracy diagnosis results

Fig 2. Proposed scan chain diagnosis in multi-EDT compression environment



Parameters	Prior art	Proposed
Diagnosis Capability	Single EDT	Multiple EDT (>2)
Need of Diagnostic Pattern Generation?	Yes	No

Reference:

1. U. Jana, S. Banerjee, B. Kumar, M. B. S. Umapathi and M. Fujita, "Deep Learning-assisted Scan Chain Diagnosis with Different Fault Models during Manufacturing Test," *2022 IEEE 31st Asian Test Symposium (ATS)*

Project 8: Extending Fault Modeling for Enhanced Test Coverage of High-speed AMS Circuits

Faculty Lead: Its open; Suraj Sindia, Intel USA

Objective:

- Develop an **advanced AFM approach** that considers structural defects, process variations, and frequency-related defect models.
- Investigate the impact of various defect models on circuit performance parameters.
- Propose efficient defect-oriented simulation flows to **reduce computational complexity** while maintaining accuracy.
- Assess the robustness of analog designs against defects and process variations.

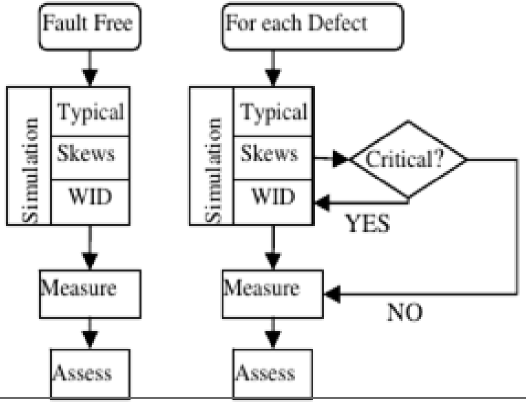
Project Goal:

- To develop a robust analog fault model
- To develop test algorithm using the proposed fault model
- To develop analog ATPG tools for IP generation

Existing Vs Proposed:

	State-of-the-art	Proposed
Simulation Time	1000 to 1500 hrs	20 to 30% reduction
Process Variation	Considered for 65nm	Lower node < 5nm

Fig 1: Existing analog test flow



Proposed Approach:

- Extend AFM to incorporate process variations and frequency-related defect models.
- Develop hierarchical simulation flows to efficiently simulate defects and process variations.
- Implement pruning algorithms to reduce computational burden without compromising accuracy.
- Analyze circuit architecture to identify critical defects and prioritize layout improvements.

Reference:

1. E. Yilmaz, A. Meixner and S. Ozev, "An industrial case study of analog fault modeling," 29th VLSI Test Symposium, Dana Point, CA, USA, 2011, pp. 178-183.
1. A Meixner and W Maly, "Fault Modeling for the Testing of Mixed Integrated Circuits", Test Conference 1991 Proceedings. International, vol. 564, 26–30 Oct 1991.

Project 9: Design and Fabrication of a Dual Mode Thermal Stress (Burn-in) Test System for Semiconductor Devices Using Indigenous Algorithm

Team: Kireetkumar D. Patel, SPU Vallabh Vidyanagar, Akshaybhai J. Patel, LCIT Mehsana

Objective:

- To investigate cyclic and constant thermal stress effect electrical behavior of semiconductor devices.
- To study degradation mechanism and contribute to scientific understanding.
- To establish industrial standards for reliability testing.

Project goal:

- To develop a testing setup with a data logging algorithm.

Proposed vs prior-art:

	Current	Proposed
Experimental design	Complex and Large	Compact Setup
Method of Experiment	Very Specific in term of thermal stress mode	Multiple thermal stress mode
Analysis	Lack of proper methodology and software	Planning to setup an analysis method using indigenous algorithm

Fig 1:Experimental Setup

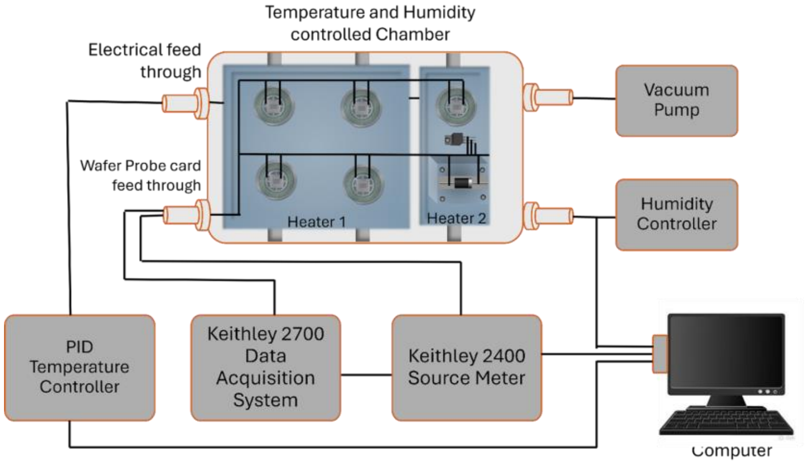
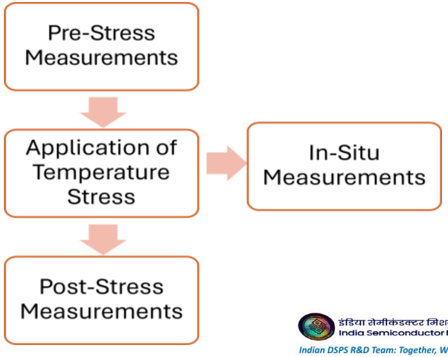


Fig 2: Mode of Operation



References:

1. **Clemmer, B.A. (2021).** *A reliability study on the effects of HTOL and high-current density stress testing on commercial-grade vertical N-type Pd/GaN Schottky diodes.* Master's thesis, Naval Postgraduate School, Monterey, California.
2. Hwang, J.; Kim, J.; Lee, J.; Cho, S.; Jeon, P. J.; Choi, S.-Y.; Kim, H. Cyclic Thermal Effects on Devices of Two-Dimensional Layered Semiconducting Materials. *Adv. Electron. Mater.* **2021**, 7 (12), 2100348. https://doi.org/10.1002/aelm.202100348.

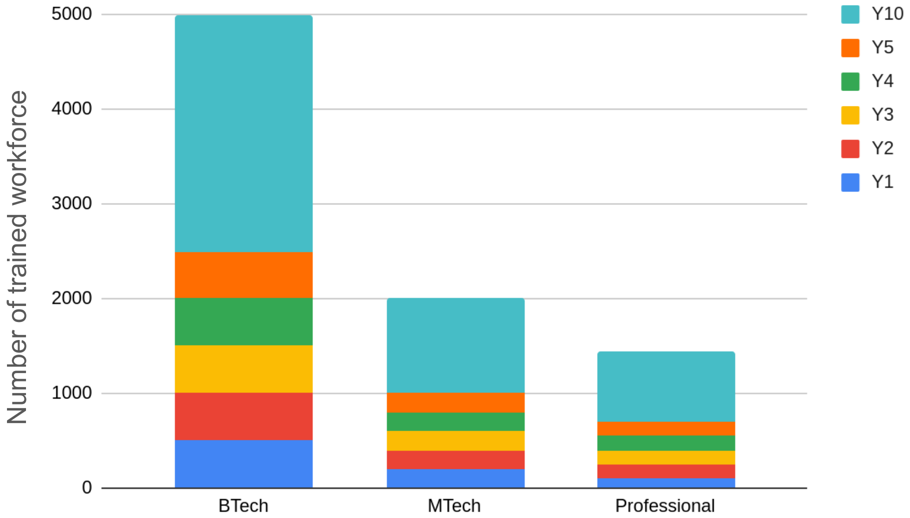
Student’s Poster for NICC

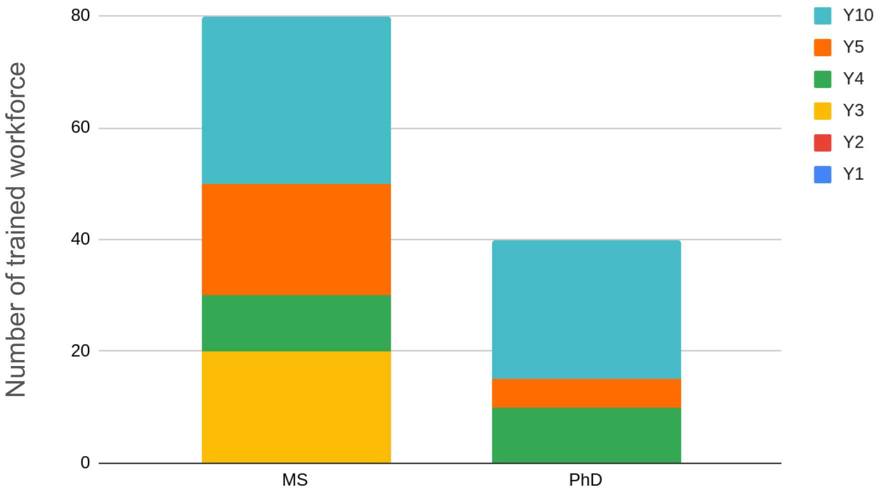
SLET-1, 2, 3, 4, 5, 6

- System level test pattern generation for systolic array [IIT Tirupati]
- High speed DFT Architecture for Chiplet SiP [IIT Tirupati]
- Side-channel resilient boundary scan architecture [IIT Jammu]
- Burn-in test architecture for semiconductor device testing [SP University]
- Layout aware Low-power Test [IIT Bombay]
- Analog Fault Modeling [Proposed by Suraj Sindia]

Educational Program: Workforce

Workforce development: BTech, MTech, Industry Professionals, MS, and PhD on System level electrical test





Program/Year	Y1	Y2	Y3	Y4	Y5	…..Y10
BTech	500	500	500	500	500	2500
MTech	200	200	200	200	200	1000
Professional	100	150	150	150	150	750
MS	0	0	20	10	20	30
PhD	0	0	0	10	5	25

Educational Program: Course/Curriculum

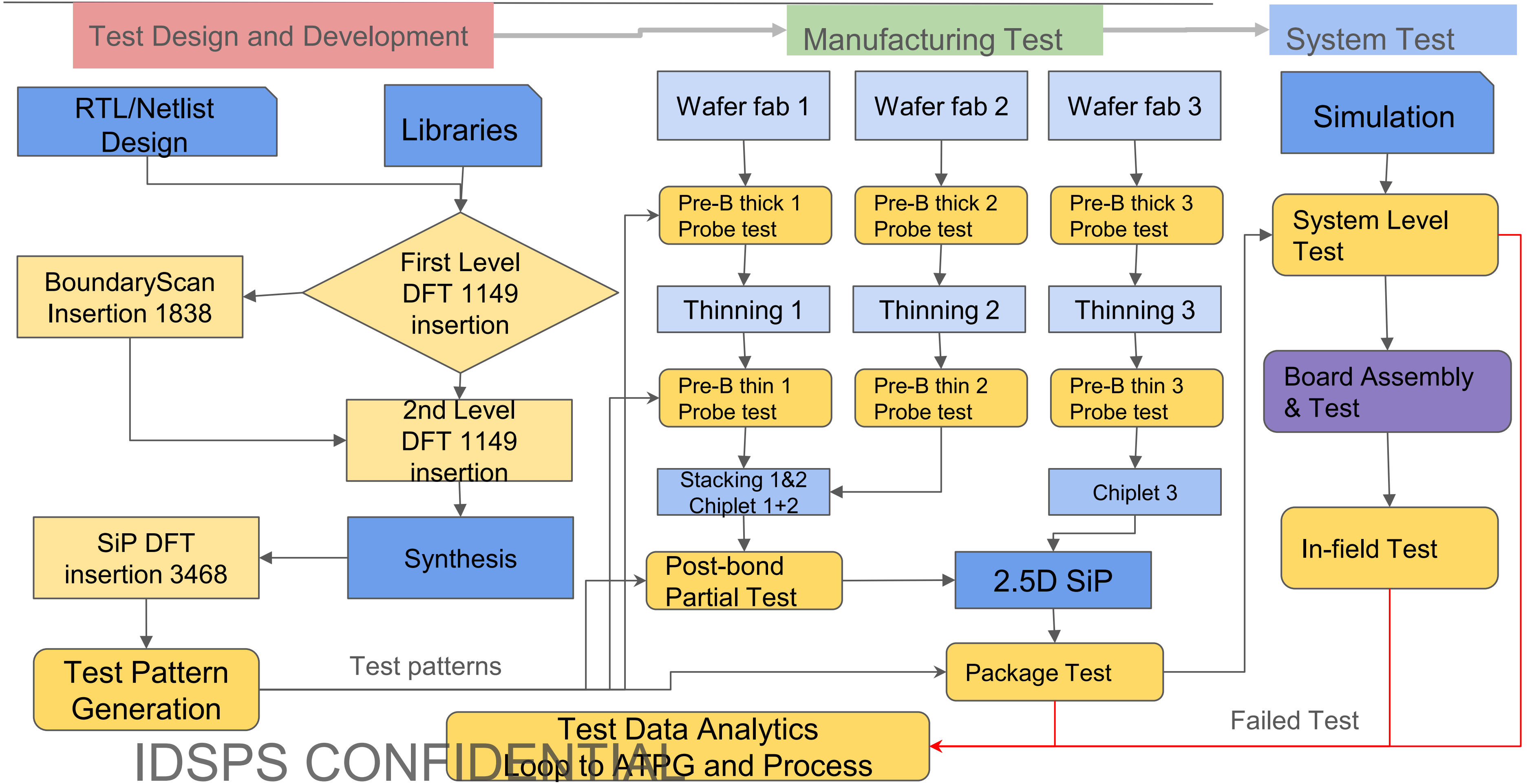
Program/Content	Content and Curriculum
Courses Duration: Semester long Credit: 2 to 4	VLSI Testing, 3D Chiplet Testing, Reliability and Fault Tolerant Design, H/W Verification and Debugging, Analog and Mixed-signal Testing, EDA tools and Algorithm, and Functional and System Level Test.
Workshop (2 per year). Duration: 1 to 2 days duration.	- Research project workshop, - System level test of chiplet, - Industry academia research workshop, - Laboratory to commercialization workshop, - Research to IP creation, - Inter SRA workshop.
Industrial Training (4 per year) - Duration: Weeklong	EDA tools: ASIC and FPGA, ATE machine bringing up, Analog measurements and data analysis, Test data analytics, Silicon life cycle management flow (SLM), FPGA prototyping, CAD tool development: Data structure, algorithm and programming in C/C++.
Skilling (4 per year) 1 to 3 days duration	Scripting - tcl, python, bash; CAD software installation and maintenance, ATE Machine operation, and Failure diagnosis.

Potential Indian and Global Companies

Company	Interest*: R&D, Workforce, Infrastructure, Technology
Qualcomm, India	R&D: False positive minimization in Test
Intel India	R&D: Functional testing and ATPG
Synopsys	Workforce: EDA Tools on Test and Verification
Teradyne	R&D and Infrastructure
Marvell	R&D: Functional Testing on ATE; Workforce: Professional development
Western Digital	R&D: DPPM Minimization in Memory Testing
Krivya Semicon	R&D: Next generation EDA tools for Test
AMD India	R&D: Power efficient APTG
Texas Instrument Siemens	R&D: Infield testing of automotive IC R&D

*The interest shown are based on informal discussion with the team members either through research paper presentation or collected from the company website

Prototyping Flow: System Level Test Flow



Infrastructure Plan: R&D Equipments

Prototyping Flow	Tools/Equipments	Cost in INR
Test Design and Development	EDA Softwares	1 Cr
	Compute workstations, Storage, and File server	2 Cr
	FPGA Prototyping boards, Peripherals - JTAG, Debugger, Analyser, Measuring instruments, and Analog Test equipments	2 Cr
Manufacturing Test	Portable ATE machines, Wafer inspection, Defect diagnosis, Outsourced ATE prober and package tester, and Maintenance cost.	2 Cr
System Level and In-field Test	System Level ATE machines, Or Outsourced ATE machines	1 Cr
	In-field test setup - Assembling boards, Measuring instruments, Host computers	1 Cr
Data Analytics	High-performance Computing, Storage, Software systems	1 Cr

Five Year Budget for ICC

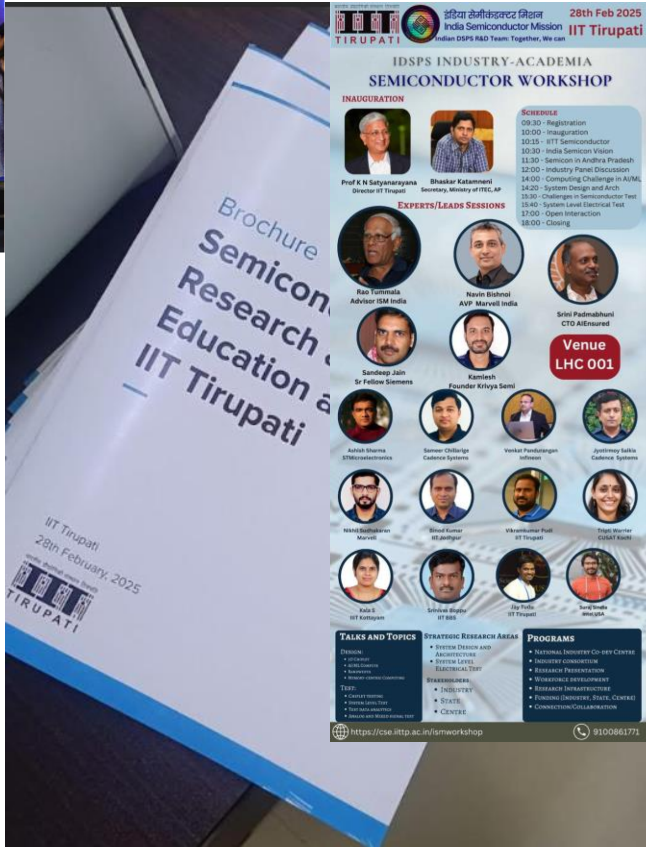
Category (Amount in INR Cr)	Row Total
1. Infrastructure Facility: 1. Equipment, 2. Installation 3. Space, Building and Cleanliness(Don't include)	10
1a. ICC Satellite (IITJ)	7.5
2. Research Projects Cost: 15 Lakhs for Design project 25 lakhs for Process project	10
3. Global Collaborators No of projects X $100K	3.36
4. Workforce Development: Workshop, Training, Courses, Seminar	1.62
4a. Workforce: Technology workforce, Manufacturing workforce PhD 40, MS 80, MTech 1000, BTech 2500, Professional 750	18
5. Personnel & Manpower for each COE	
Full-Time Research Faculty	2.65
Company Engineers on Campus	0.27
Maintenance Staff	0.48
Manager of Operations	1.2
COE Secretary	0.48
Financial	0.48
6. Travel: Travel to Companies and Conferences	0.6
Column Total	**~60 Cr**

Five Year Milestone

Deliverables	Year 1		Year 2		Year 3		Year 4		Year 5	
Formation of industry consortium	■	■								
Equipment procurement and Installation	■	■	■	■	■	■				
Definition of projects (detailing)	■	■								
Workforce training MS/PhD/MTech/BTech	■	■	■	■	■	■	■	■	■	■
Workforce training Professionals		■	■	■	■	■	■	■	■	■
Setup of Primary and Secondary ICC on Test		■	■	■						
Training and Skilling facilities setup		■	■	■	■	■				
Technology Demonstration and Development					■	■	■	■		
Design and Demonstration of Prototype							■	■	■	■
Technology Licensing and IP Generation									■	■

*The workforce training for BTech, MTech, MS, and PhD shall continue upto 10th years the project.
*Project completion time varies between 2 to 3 years.

Call for Collaboration



IIT Tirupati &
IIT Jammu

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Open for Discussion

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Thank You