Next-gen Power Devices

Industry Co-development Centre with National Industry Consortium for Next-gen Research and Workforce

Akshay K, IIT Bhubaneswar (Lead)
Ankush Bag IIT Guwahati (Co-lead)
P V Satyam, IIT Bhubaneswar (Co-lead)
Vijaya Kumar (IIT TP), Arvind Ajoy (IIT Pkd)
Abhinav Arya (IIT BBS), P K Tyagi (DTU)

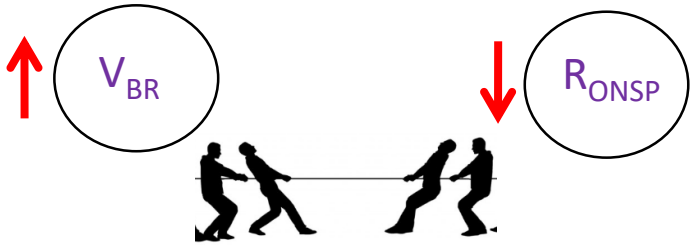
Guru Thalapaneni, SiCSem (Industry Lead)

Global academic collaborator
Prof. Anant Agarwal, Ohio State University, U.S.A

Global research collaborator
Dr. Sudhiranjan Tripathy, IMRE, A*STAR, Singapore

Advisor
Prof. Shreepad Karmalkar, IIT Bhubaneswar

Next-Gen Industry Needs and Technical Challenges



Conventional Design Trade-off

1. On-state
- R_{ONSP}
- V_T
- $I_{DS,sat}$

2. Blocking / Off-state
- V_{BR}
- I_{off}

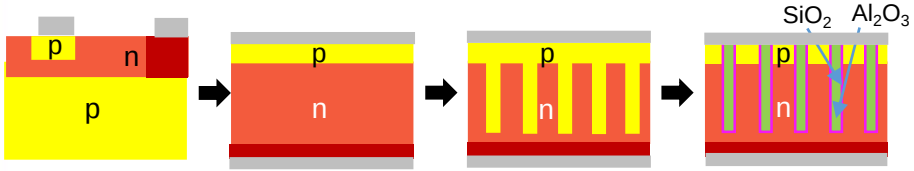
3. Switching performance
- Q_g, C_{iss}
- C_{gd}, C_{oss}
- E_{on}, E_{off}
- Q_{rr}

4. Thermal performance
- $R_{\theta,jc}$, $R_{\theta,ja}$
- Safe operating area
- dR_{on}/dT

5. Reliability Tests
- UIS (I_{av}, E_{as}, E_{ar})
- SC Test (t_{SC})
- TDDB
- HTRB
- HTGB
- SEB/SEGR
- ESD Tests

Innovations in power devices can be broadly categorized into two:

1) Structural/Process level innovations e.g. drift layer



Lateral 1-D Junction | Vertical 1-D junction | Super-Junction (SJ) | Charge Sheet Super-Junction (CSSJ)

Focus Area: Discrete/integrated devices with 1-D / charge coupled drift layer

2) Material level innovations

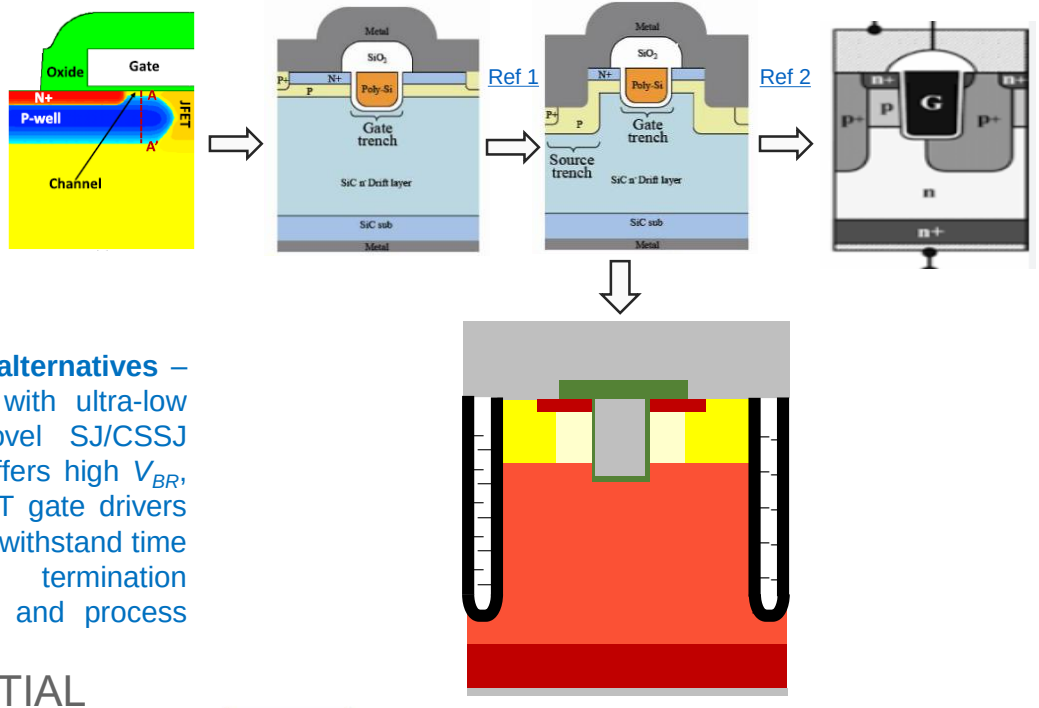
Silicon ➡ Silicon Carbide GaN ➡ Ga_2O_3 Diamond AlN

Focus Areas:
- Large area SiC wafer (8”)
- Electronic grade WBG and UWBG materials
- Si, WBG and UWBG devices and integrated modules

Research Vision: Current vs. Proposed Approach

Alternate device structures could address existing challenges

e.g. Prior Art in SiC



One of the proposed alternatives – SiC Trench MOSFET with ultra-low R_{ONSP} (no JFET), novel SJ/CSSJ based drift layer that offers high V_{BR}, compatible with Si IGBT gate drivers due to high short circuit withstand time and robust edge termination insensitive to humidity and process variations.

Multidisciplinary India-wide Faculty Team with Expertise in Strategic Areas

Dr. Akshay K
IIT Bhubaneswar
Device design and fabrication

Prof. S Karmalkar
IIT Bhubaneswar
Device design and fabrication
Power Devices Technology

Prof. P V Satyam
IIT Bhubaneswar
Substrate/epi growth and characterization

Dr. Abhinav Arya
IIT Bhubaneswar
Devices testing and failure analysis

Dr. Vijaya Kumar G
IIT Tirupati
Device modeling and simulation

Dr. Arvind Ajoy
IIT Palakkad
Device characterization

Dr. Ankush Bag
IIT Gandhinagar
GaN & Ga_2O_3 device fabrication

Dr. P K Tyagi
DTU
Substrate and epi growth (diamond)

Research Vision: Strategic Research Focus Areas And Faculty Leads

e.g. 0.6–1.2 kV Class SiC Trench MOSFETs (with SJ/CSSJ drift layer) Having Ultra-Low R_{ONSP}

(3) Device design

- High short circuit withstand time, low conduction and switching losses, robust edge termination, immune to process variation, temperature & humidity

- Akshay and S Karmalkar IIT BSS

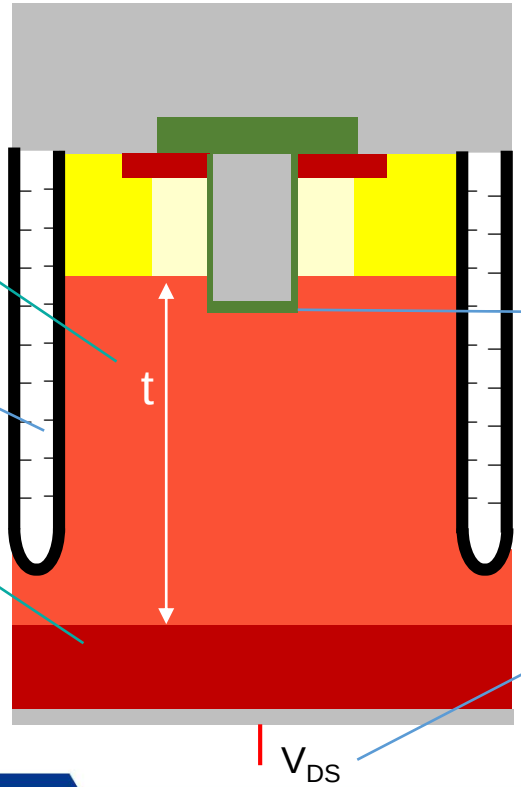
(2) Simulation and modeling

- comprehensive multidimensional approach, compact modeling for system level performance assessment

- Vijay IIT T

(1) Substrate and epi growth

- electronic grade large area wafer, dicing, polishing, a- & c-axis growth for anisotropic impact ionization coefficient studies
- Satyam IIT BBS (SiC, GaN, diamond)
- S Karmalkar IIT BBS (SiC)
- P K Tyagi, DTU (diamond)
- S Tripathi (A*STAR)



(4) Device fabrication

- contact resistance and gate work function optimization, other process recipe optimization.

- Akshay, Avijit & Karmalkar IIT BSS SiC
- Ankush IIT G, GaN, Ga2O3

(5) Device testing and failure analysis

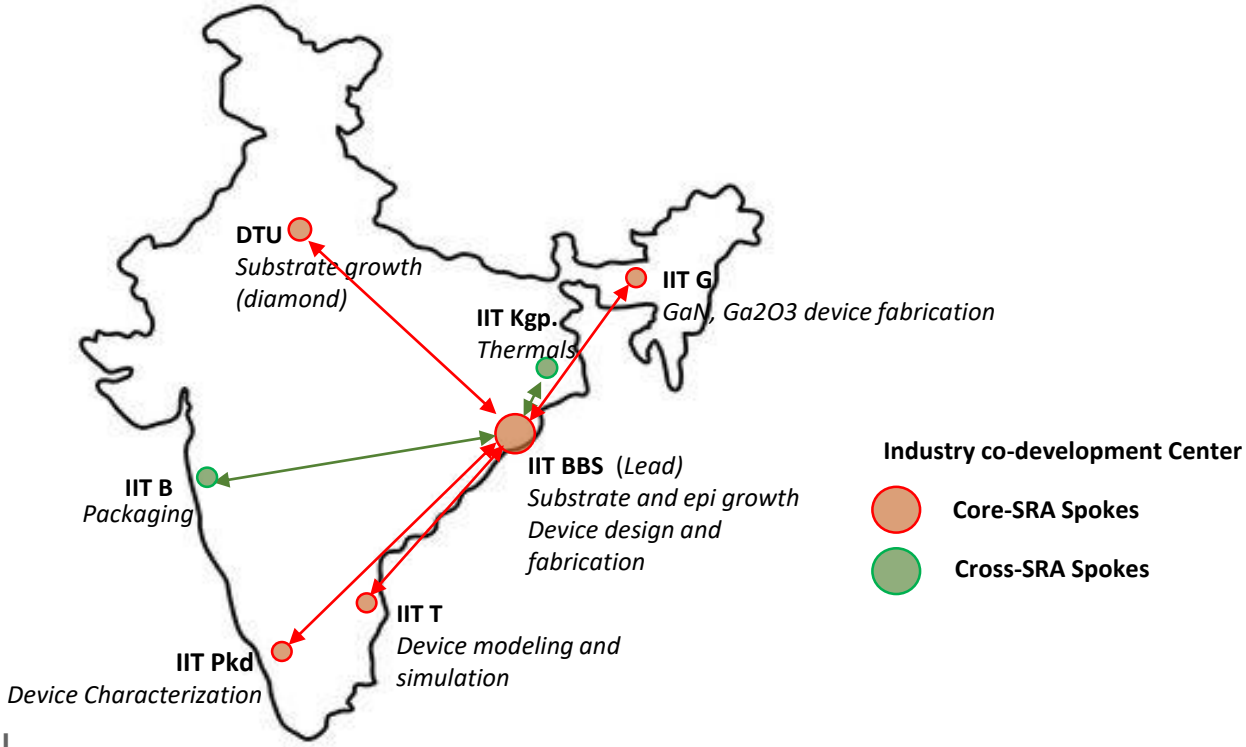
- Condition monitoring
- Lifetime improvement,
- device and package level degradation mechanism, SEM imaging
- Abhinav IIT BSS
- Satyam IIT BBS

(6) Device characterization

- I-V, C-V, switching performance (DPT), avalanche robustness (UIS)

- Arvind, IIT Pkd

Hub & Spoke Model of the Power Devices ICC



Industry Partners

Interested Companies

SiCSem

RUTTONSHA

iVP SEMI

nano semic

CDIL

MELSS

PIB
https://pib.gov.in › PressReleaseIfra...

SiCSem to collaborate with IIT Bhubaneswar for building the Compound Semiconductor ...

15 Jun 2024 — The first project to be carried out as part of this agreement would indigenize Silicon Carbide (SiC) crystal growth at IIT Bhubaneswar.

Potential Partners (having operations in India)

Infineon

ROHM SEMICONDUCTOR

RENESAS

NXP

onsemi

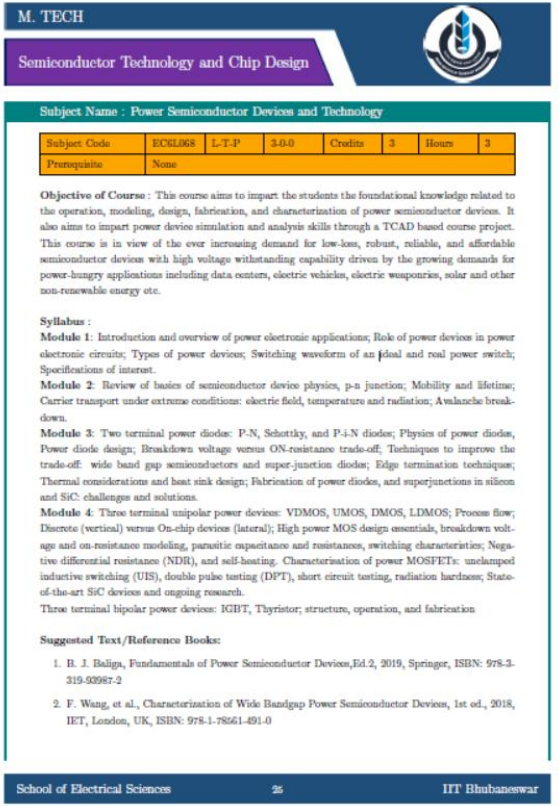
Technology workforce education programs

- **Short-term (1 year):**
  - Already implemented
    - Power Semiconductor Devices and Technology course for B.Tech, M.Tech, and Ph.D.
    - B.Tech. in Engineering Physics (with Power Semiconductor Devices and Technology as elective).
  - Develop graduate-level theory course on substrate and epi-growth of wide bandgap semiconductors.
  - Knowledge acquisition: webinars, in-person expert workshops

- **Long-term (5-10 years):**
  - **Educated workforce target (over 5 years) – B.Tech: 300, M.Tech: 150, Ph.D. : 25**
  - **Educated workforce target (over 10 years) – B.Tech: 700, M.Tech: 400, Ph.D. : 60**
  - Hands-on lab for students (B.Tech, M.Tech, Ph.D. and PDC)/ industry professionals on design, fabrication, characterization, and testing at IIT Bhubaneswar and upcoming fabs in Bhubaneswar.
    - e.g., TCAD, analytical device design, clean room training, device fabrication, use of probe station & curve tracer, characterization to obtain I-V, C-V and switching data, failure testing and quality control.
  - Month-long hands-on training of M.Tech and Ph.D. students at US and Singapore collaborating institutions.

Power Semiconductor Devices and Technology Course @ IIT Bhubaneswar

- For B.Tech, M.Tech, and Ph.D.
- Students from EE, ECE, MM, and ME
- Live demo of a power electronic circuit
- Showcasing different power devices
- Datasheet discussion integrated into lectures
- Few datasheet based assignments and exam questions



M. TECH

Semiconductor Technology and Chip Design

Subject Name : Power Semiconductor Devices and Technology

Subject Code	EC6L068	L-T-P	3-0-0	Credits	3	Hours	3
Prerequisite	None						

Objective of Course : This course aims to impart the students the foundational knowledge related to the operation, modeling, design, fabrication, and characterization of power semiconductor devices. It also aims to impart power device simulation and analysis skills through a TCAD based course project. This course is in view of the ever increasing demand for low-loss, robust, reliable, and affordable semiconductor devices with high voltage withstanding capability driven by the growing demands for power-hungry applications including data centers, electric vehicles, electric weaponries, solar and other non-renewable energy etc.

Syllabus :

Module 1: Introduction and overview of power electronic applications; Role of power devices in power electronic circuits; Types of power devices; Switching waveform of an ideal and real power switch; Specifications of interest.

Module 2: Review of basics of semiconductor device physics, p-n junction; Mobility and lifetime; Carrier transport under extreme conditions: electric field, temperature and radiation; Avalanche breakdown.

Module 3: Two terminal power diodes: P-N, Schottky, and P-i-N diodes; Physics of power diodes, Power diode design; Breakdown voltage versus ON-resistance trade-off; Techniques to improve the trade-off: wide band gap semiconductors and super-junction diodes; Edge termination techniques; Thermal considerations and heat sink design; Fabrication of power diodes, and superjunctions in silicon and SiC: challenges and solutions.

Module 4: Three terminal unipolar power devices: VDMOS, UMOS, DMOS, LDMOS; Process flow; Discrete (vertical) versus On-chip devices (lateral); High power MOS design essentials, breakdown voltage and on-resistance modeling, parasitic capacitance and resistances, switching characteristics; Negative differential resistance (NDR), and self-heating. Characterisation of power MOSFETs: unclamped inductive switching (UIS), double pulse testing (DPT), short circuit testing, radiation hardness; State-of-the-art SiC devices and ongoing research.

Three terminal bipolar power devices: IGBT, Thyristor; structure, operation, and fabrication

Suggested Text/Reference Books:

1. B. J. Baliga, Fundamentals of Power Semiconductor Devices,Ed.2, 2019, Springer, ISBN: 978-3-319-93987-2
2. F. Wang, et al., Characterization of Wide Bandgap Power Semiconductor Devices, 1st ed., 2018, IET, London, UK, ISBN: 978-1-78561-491-0

School of Electrical Sciences 25 IIT Bhubaneswar

Facilities Available at IIT Bhubaneswar

S.No	Description	Status	Funding
1	Clean rooms (Class 10 k: 83 m^2 and 1 k: 40 m^2)	Operational	**IITBBS – DST FIST**
2	Clean Room: Class 100 (30 m^2) CMP, Defect Inspection, KoH etc	Operational	**SiCRIC**
3	Crystal Growth – PVT (8 inch furnaces) for SiC boule, OD Grinder	Operational	**SiCRIC**
4	Multi Wire Saw	Expected soon	**SiCRIC**
5	Wafer inspection: Resistivity mapping Boule resistivity measurement	Operational soon	**SiCRIC**
6	Probe Station, Mask Aligners, Metallization	Available	**IITBBS**
7	SEM, FEGSEM	Available	**IITBBS**
8	Packaged device holder and IV tester with integrated thermal chamber	Available	**IITBBS + ANRF**
9	TCAD Tools and Workstations	Available	**C2S + IITBBS + ANRF**

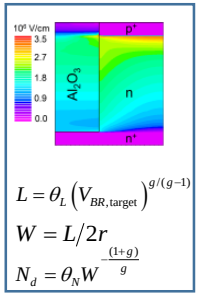
Infrastructure: Process Flow and Tools

SiC seed → 8” SiC boule → 8” SiC wafer

- for GaN devices: Buffer / GaN / nucleation / SI
  - metrology: TEM, AFM, PL, XRD, Raman
- for SiC Devices: SiC epi-layer / n^+
  - MOCVD (GaN), MPCVD (diamond)

PVT (industry supported) ← Slicing + polishing (industry supported) ← epilayer growth (industry supported) ← No

* Process flow is illustrated only for a novel diode (CSSJ). Similar flow can be made for MOSFETs & other devices.



Simulation + Modeling

Lithography, FIB SEM, D-RIE, Implantation

Oxidation Furnaces (SiO_2 liner)

ALD (Al_2O_3)

CVD, CMP (dielectric)

Sputtering, RTA, Metallization (Schottky)

Characterization → Testing → Meets Spec ?

Yes → Next Gen Power Devices

Next Gen Specs from Industry

Proposed List of R&D projects with Faculty Leads for Each

1. Compound semiconductor materials development including SiC, GaN, Diamond, AlN, GaOx, high purity Graphite, and related equipment design and prototype production.
   Prof. Satyam (IIT BBS), **Prof. S Karmalkar (IIT BBS),** Dr. Sudhiranjan (A*STAR), Guru (SiCSem)
2. Device-Circuit Co-optimization of Superjunction Devices.
   Dr. Vijay (IIT T)
3. Compact Modelling of Power Devices for Accurate Simulation of Power Converters.
   Dr. Vijay (IIT T)
4. Development of Charge Sheet Superjunctions in Silicon and SiC Materials
   Dr. Akshay (IIT BBS), Prof. Karmalkar (IIT BBS), Prof. Satyam (IIT BBS), Dr. Vijay (IIT T) Dr. Sudhiranjan (A*STAR)
5. Design and Development of Diamond Schottky Barrier Diodes
   Dr. Akshay (IIT BBS), Prof. Karmalkar (IIT BBS)
6. Characterization of Next Generation SiC/GaN/Ga_2O_3/Diamond Power Devices Using In-House Testing Equipment
   Dr. Arvind (IIT Pkd)
7. Investigation of Failure Mechanisms in SiC and GaN Power Modules with Advanced Packaging Technologies
   Dr. Abhinav (IIT BBS) and Dr. Akshay (IIT BBS)
8. Lifetime Improvement and Condition Monitoring of SiC and GaN Power Devices for EV Applications
   Dr. Abhinav (IIT BBS) and Dr. Akshay (IIT BBS)
9. Development of Vertical GaN Technology for kV-Class Power Devices
   Dr. Ankush (IIT G) and Guru (SiCSem)
10. Development of Gallium Oxide Technology for High Power Applications
    Dr. Ankush (IIT G) and Guru (SiCSem)

Thank You

Email ID: akshay@iitbbs.ac.in

Project 1: Compound semiconductor materials development including SiC, GaN, Diamond, AlN, GaOx, high purity Graphite, and related equipment design and prototype production.

Team: P V Satyam (IITBBS), S Karmalkar (IITBBS) P K Tyagi (DTU), Dr Sudhiranjan Tripathy (IMRE, Singapore), SiCSem

Objectives:

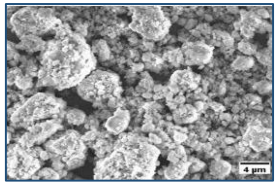
- Design, fabricate, test and qualify the Reactors/Furnaces for
  - 300 mm diameter SiC substrate for SiC devices. a- and c-axis growth for studying anisotropic impact ionization coefficients using PL and EBIC.
  - 200 mm diameter Semi insulating SiC as substrates for HEMT
- Design, fabricate and certify the Microwave CVD for electronic grade diamond growth
- Make a seed for 50 mm diameter wafer grade diamond using Zr/Ir/Diamond films

Proposed vs. Prior Art:

- 300 mm diameter SiC technology not available in India. Import restrictions worsen this problem.
- 50 mm diameter electronic grade diamond technology not available until now.

This is needed for our nations' strategic purposes

Approach for SiC Substrates:



Devise methods to make 99.9999% or better SiC powders – used as source.

- Select seed available
- Optimize Growth process
- Grow SiC Crystal
- Slice into Wafers
- Validate the electronic grade quality

50 mm Diamond Substrate

Indigenous MPCVD system

Defect inspection techniques

Quality assurance

Project 2: Device-Circuit Co-optimization of Superjunction Devices

PI: Gurugubelli Vijaya Kumar (IIT Tirupati)

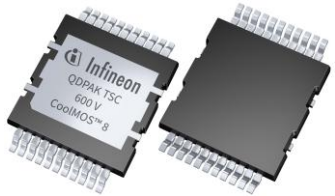
Objective: To develop analytical models for the design of an optimized superjunction power MOSFET in view of typical operating conditions encountered in a circuit.

Potential applications: Prime focus on EV- Onboard automotive chargers, power factor correction (PFC) boost converter stage, etc.

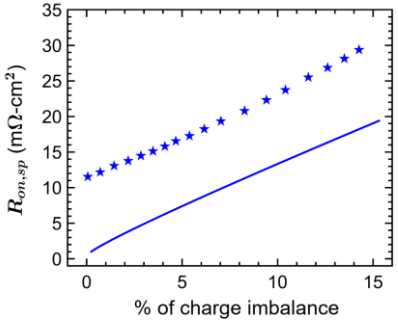
Current status	Proposal
• Analytical models for the optimization to achieve the best possible trade-off between breakdown voltage and on-resistance. • Comprehensive analysis of switching conditions and capacitances.	• Modeling and optimization of power losses including on- resistance, capacitances and circuit operating conditions. • Involves analysis of on-state, off-state and transients.

Considerations:

- Commercial devices thrive on improving the dv/dt capability and better unclamped inductive switching (UIS) behavior.
- Optimization problem now includes: breakdown voltage capability, specific on-resistance minimization, low gate charge and parasitic capacitance.



600 V CoolMOS™ 8 SJ MOSFET family for advanced and cost-effective power supply applications - Infineon Technologies



Proposed theoretical lowest limit of silicon SJ specific on-resistance, till date. Line: Our model; Symbols: W. Saito 2015 IEEE 27th ISPSD, 2015, pp. 125-128.

Project 3: Compact Modelling of Power Devices for Accurate Simulation of Power Converters

PI: Gurugubelli Vijaya Kumar (IIT Tirupati)

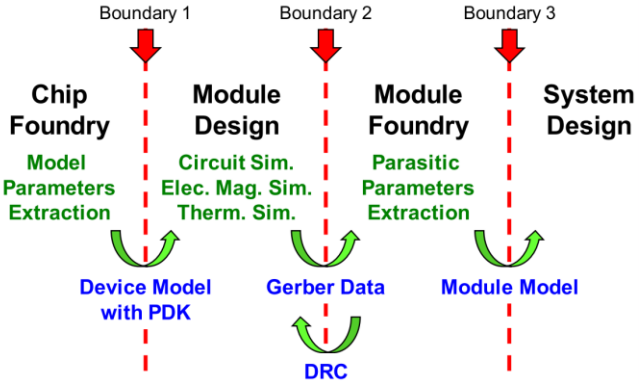
Objective: To develop physics-based compact models for power devices that can be used in circuit simulations

Current status:

- Matured models for LDMOS are available for circuit simulations.
- Models for unipolar devices like SiC power MOSFETs, GaN HEMTs are reasonably advancing.
- Existing models for SJ power MOSFETs or bipolar devices like IGBTs and FWDs are primitive and behavioral.

Proposal:

- Necessity for accurate physics-based model
- We aim to provide physics-based models in conjunction with behavioral models, as necessary, targeting SJ power MOSFETs, IGBTs and FWDs



W. Saito, "A Future Outlook of Power Devices From the Viewpoint of Power Electronics Trends," in *IEEE Transactions on Electron Devices*, vol. 71, no. 3, pp. 1356-1364, March 2024.

Considerations:

- Compact semiconductor device modeling involves (1) development of a generic physics-based model, (2) implementation of the model into a circuit simulator, (3) development of a simple parameter extraction sequence, and (4) model validation.
- Operating conditions can include a range of temperatures, dv/dt's, di/dt's, current and voltage levels.

Project 4: Development of Charge Sheet Superjunction in SiC

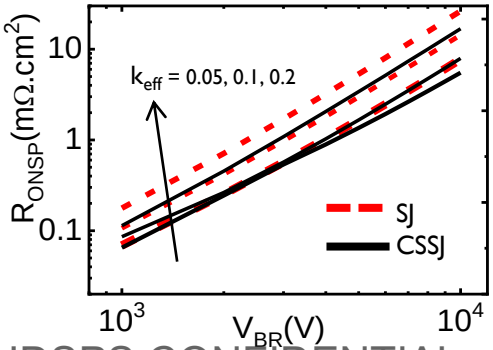
PI: Akshay K (IITBBS)

Co-PIs: Prof. Karmalkar, Prof. Satyam (IITBBS), Vijay (IIT T), Dr. Sudhiranjan (A*STAR, Singapore)

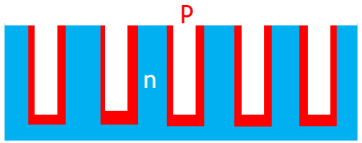
Objectives

Design and develop a viable alternative to superjunction in SiC material.

SiC superjunction not commercially viable



Prior Art



Conventional Super-Junction

Multiple straight and tilted implants

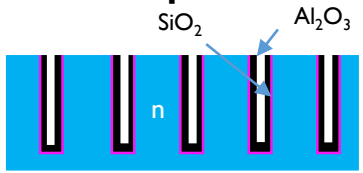
1) Multiple high energy implantations: Expensive

2) Controlled p-dopant activation difficult : larger charge imbalance

3) Wide trench : higher R_{ONSP}

4) Limit in trench depth: limits the V_{BR}.

Proposed



Charge Sheet Super-Junction

Trench is lined with SiO_2 and Al_2O_3

1) No high energy implantation.

2) No p- pillar. Lower charge imbalance.

3) SiC technology allows $W_l < W_p$.

4) No severe limitation in trench depth. Conformal deposition achieved for aspect ratio up to 50

Facility Required

- Inductively Coupled Plasma RIE (ICP-RIE)
- Implanter (termination)
- Metallization

References

1) K. Akshay et.al., "Charge Sheet Super Junction in 4H-Silicon Carbide: Practicability Modeling and Design", IEEEJ. Electron Devices Soc., vol. 8, pp. 1129-1137, 2020.

2) X. Zhong et.al., "Experimental Demonstration and Analysis of a 1.35-kV 0.92-mΩ.cm2 SiC Superjunction Schottky Diode", IEEE TED, vol. 65, no.4, pp.1458-1465, 2018.

Project 5: Design and Development of Diamond Schottky Barrier Diodes

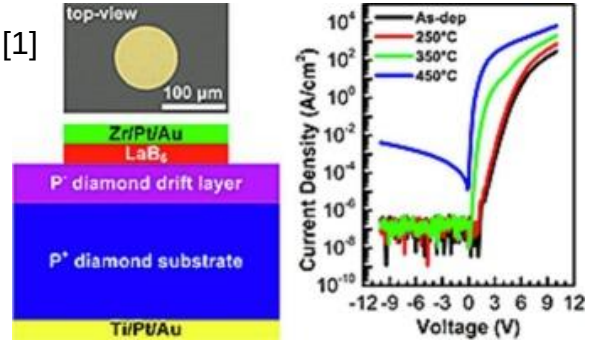
PI: Akshay K (IITBBS)

Co-PIs: Prof. Karmalkar (IIT BBS)

Objectives

- Design and develop diamond Schottky barrier diodes (SBDs) with ultra-high breakdown voltage, low on-resistance, and excellent thermal stability, thereby unlocking diamond's potential for next-generation power electronics.

[1]



Prior Art

Si and SiC SBDs: Mature technologies but limited by bandgap (~1.1 eV for Si, 3.2 eV for SiC) and thermal conductivity (< 5 W/cm·K).
GaN SBDs: High electron mobility but challenges in thermal handling and vertical scalability.
Diamond devices: Offer extreme material properties (bandgap 5.5 eV, breakdown field ~10 MV/cm, thermal conductivity > 20 W/cm·K), but : Difficulty in **achieving low-resistance ohmic contacts**.
High Schottky barrier heights that increase forward voltage drop.
Limited reproducibility of doping and surface passivation techniques.

Proposed

1. Optimized Schottky contact selection and barrier engineering
2. interface engineering; reducing defects, leakages
3. Novel device architectures

Facility Required

- Lithography and metallization unit
- Furnaces for annealing, passivation
- Implanter

References

[1] G. Shao et.al., "Effect of rapid thermal annealing on performances of vertical boron-doped diamond Schottky diode with LaB_6 interlayer," Diamond Relat. Mater., vol. 132, art. no. 109678, 2023.
[2] V. D. Blank, et.al., "Thin large-area vertical Schottky barrier diamond diodes with low on-resistance made by ion-beam assisted lift-off technique," Diamond Relat. Mater., vol. 75, pp. 78–84, 2017.

Project 6: Characterization of Next Generation SiC/GaN/Ga2O3/Diamond Power Devices Using In-House Testing Equipment

PI: Prof. Arvind Ajoy, IIT Palakkad

Objective:

- To develop an indigenous device characterization equipment suitable for IV tracing, Double Pulse Testing (DPT) and Unclamped Inductive Switching (UIS) in a compact form factor.
- Analyze the power switch characteristics at different corner conditions and temperature ranges.

Proposed Approach:

- A test equipment with controllable pulses and adjustable temperature is used to simulate various working conditions of the DUT to analyze the performance of the DUT.
- Dedicated high current (Rogowski coil based) and high voltage measurement circuitry with focus on reducing the inductive effects in probing and higher accuracy.
- 2 channel 24bit ADC based data-acquisition system with high sampling rate and processing is carried in custom-made GUI in personal computer.
- The high voltage for testing to be provided external to the proposed testing set-up.

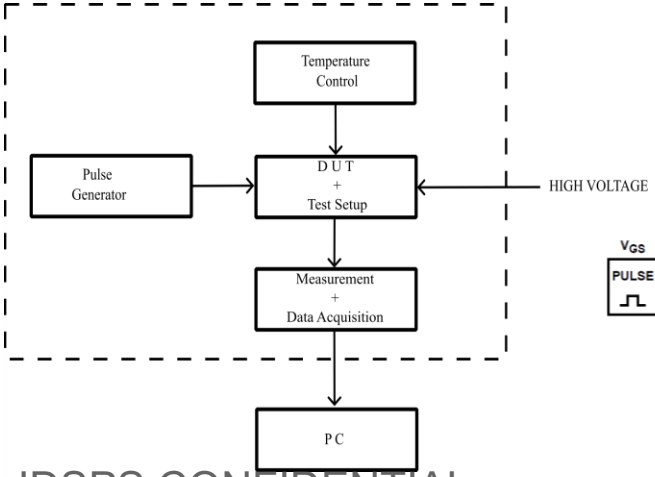
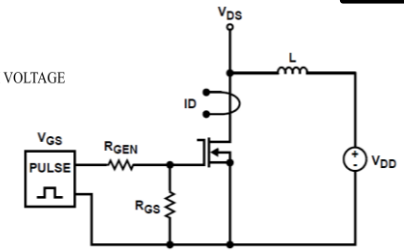
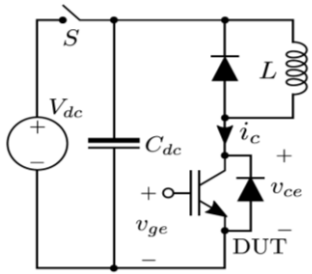


Fig. Proposed block diagram of the characterization set-up.



Test set-up for UIS of DUT



Test set-up for DPT of DUT

References:

[1]. Renesas - Application note - Unclamped Inductive Testing

[2]. Double Pulse Testing: The how, what and why?

[3]. Double Pulse Testing - Hardware Design and Measurement Guidelines

Project 7: Investigation of Failure Mechanisms in Next Generation SiC and GaN Power Devices for EV Drive Applications

PI: Abhinav Arya (IITBBS)

Co-PIs: Akshay K. (IITBBS)

Objectives

- Identifying critical failure modes in new generation SiC power devices for EV inverters
- Identifying key electrical/thermal parameters showing strong coupling with device degradation

New generation SiC power devices

Current status [1] – [3]

- Improvising chip designs
  - Reduction in power losses
- Modifying packages
  - New materials and technology
  - Reduced parasitic inductances
- Thermal cycling

Proposal

Reliability assessment

- Chip and package level degradation evaluation
- Effect of multiple stressors like temperature, humidity and vibrations
- Aggressive stress profiles in EVs - a reliability critical application

Test bench development for emulated real time loading

- Implementing transient driving cycles
- Considering different new technology devices
- Operation under different stress conditions

Key stressors

Ambient Temperature, Humidity and Vibrations

Monitoring of parameters

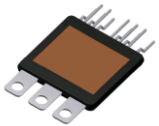
- Identification of suitable electrical and thermal parameters
- Static and dynamic characterization of devices
- Parameters measurement setup

Analyzing obtained parameters and SEM images

- Degradation type: chip/package and location
- Level: changes in parameters
- Criticality: linking parameters to degradation fatality through SEM images

Critical degradation mechanisms

Microsemi extremely low inductance SP6LI package SiC MOSFET Power Modules (MSCSM70AM025CT6LIAG)



Infineon double side cooled IGBT module (FF400R07A01E3_S6)

Wolfspeed new generation SiC half bridge module (CAB006A12GM3)

SEMICRON DANFOSS: Molded module packaging with fully sintered SiC MOSFETs

[1] H. Lee, et al., "A Review of SiC Power Module Packaging Technologies: Challenges, Advances, and Emerging Issues," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 239-255, March 2020
[2] F. Yang, et al., "Electrical Performance Advancement in SiC Power Module Package Design With Kelvin Drain Connection and Low Parasitic Inductance," in IEEE Journal of Emerging and Selected Topics in Power Elect., vol. 7, March 2019
[3] https://www.meu-semiconductor.eu/wp-content/uploads/2022/04/Bodos-Power-Systems_19-09_Mitsubishi-Electric-Semiconductor.pdf

Project 8: Lifetime Improvement and Condition Monitoring of Next Generation SiC and GaN Power Devices for EV Applications

PI: Abhinav Arya (IITBBS)

Co-PIs: Akshay K. (ITBBS)

Objectives

- Enhanced lifetime through Active Thermal Control (ATC)
- Real-time health status through condition monitoring (CM)

Current status [1] – [3]

Methods limited to

- Si based power devices
- Standard packages
- Some applications like solar inverters etc.

Proposal

Advance methods for

- Next generation SiC power devices
- EVs – a reliability critical application

Lifetime improvement by Active Thermal Control

Electrical methods of equalizing and minimizing thermal stresses on SiC power devices

Optimization of lifetime and efficiency of devices

Implementation of proposed ATC method on actual converter

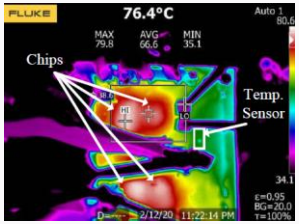


Fig. Thermal image of de-capsulated power module (top) showing inside temperature distribution during its application (captured using FLUKE IR camera)

Identify critical failure modes

Identify suitable Health Sensitive Electrical Parameter (HSEP) and its measurement

Experimentation for characterization of HSEP

Online remaining useful lifetime estimation of devices

Real-time health status through condition monitoring

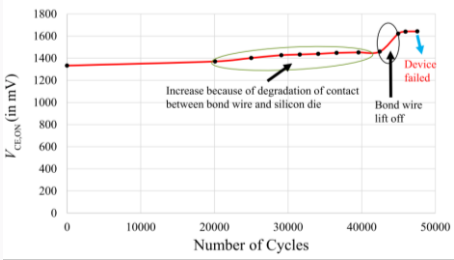


Fig. Example showing on-state voltage monitoring method to estimate bond-wire degradation in IGBT [1]:

[1] A. Singh, et al., "Evaluation of Vce at Inflection Point for Monitoring Bond Wire Degradation in Discrete Packaged IGBTs," in IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 2481-2484, April 2017
[2] A. Chandhar, N. Deshmukh, A. Arya and S. Anand, "Gate Voltage-Based Active Thermal Control of Power Semiconductor Devices," in IEEE Transactions on Power Electronics, vol. 38, no. 9, pp. 11531-11542, Sept. 2023
[3] Z. Ni, et al., "Overview of Real-Time Lifetime Prediction and Extension for SiC Power Converters," in IEEE Transactions on Power Electronics, vol. 35, no. 8, pp. 7765-7794, Aug. 2020

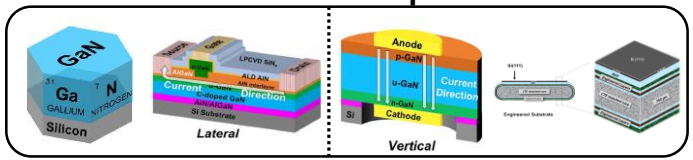
Project 9: Development of Quasi-Vertical GaN Technology for kV-Class Power Devices

PI: Ankush Bag (IITG)
Co-PI: Guru Thalapaneni (SiCSem)

Objectives:

a) Development of quasi-vertical GaN devices with improved junction termination for enhanced power handling capabilities.
b) Monolithically Integrate GaN power components seamlessly with drivers.
c) Enhance the reliability and durability of GaN devices, including bidirectional switches.
d) Grow thick GaN epitaxial layers on silicon-engineered substrates with enhanced thermal conductivity
e) GaN on Sapphire on a larger diameter wafer

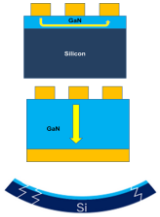
Prior Art vs Proposed



	Existing	Purposed
Device Architecture	Lateral Devices	Vertical Devices
Rated Voltage	650 V	1200 V
Integration	Composite Devices	Monolithic
Substrate used	Silicon, Sapphire etc.	Engineered Substrate (QST)
Thermal coefficient mismatching	High	Low due to QST
Reliability & Robustness	Great Challenge	Better, due to thick drift layer

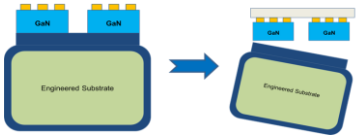
Proposed Approach

Challenges with silicon substrate



- Currently lateral devices are mostly explored in GaN.
- Vertical power devices require 10 micron or more high quality epilayer.
- Thick growth without native substrate leads to Cracks in the layer.

Using Engineered Substrates



- Engineered substrate enables high quality crack free Thick GaN.
- Substrate can be reused by transferring the devices.
- Better device performance expected.

- Vertical devices with thick, high quality GaN material compatible to Silicon foundry.
- large area wafer (12 inch or more) to have better yield/ throughput.

Facility Required

- Inductively Coupled Plasma RIE (ICP-RIE)
- Metal organic chemical vapor deposition (MOCVD) / Molecular beam epitaxy (MBE)

Outcome and Impact

These technologies will further extend the power device's performance, along with improved reliability and durability, at a lower cost.

[1]- *Fundam. Res. 2022,2(3),462–475* [2]- *WiPDA ,2019,292-296* [3]- *IEEE TPEL,2023, 38(7), 8442-8471*

Project 10: Development of Gallium Oxide Technology for High Power Applications

PI: Ankush Bag (IITG)
Co-PI: Guru Thalapaneni (SiCSem)

Objectives –

a) Develop vertical Gallium oxide based power diodes with lower on-resistance and high breakdown Voltage.
b) Use of P and N type doping to achieve PN junction termination.
c) Grow thick Gallium oxide epitaxial layers on Native or Sapphire substrate with a larger diameter.

Proposed Approach

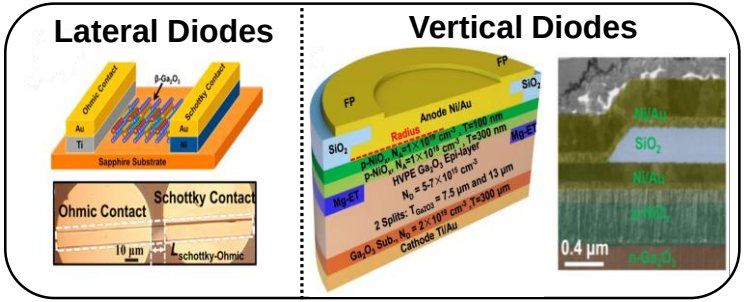
- ❑ Realize the P type Gallium oxide on lightly doped N-type Gallium oxide.
- ❑ Combination of other P type oxides like NiO_x to realize the vertical PN heterojunction Diodes.
- ❑ Optimize the epilayer on larger diameter wafer size to have higher yield.

Facility Required

- Metal organic chemical vapor deposition (MOCVD)
- Inductively Coupled Plasma RIE (ICP-RIE)

[1]- Zhang, J., Dong, P., Dang, K. *et al.* Ultra-wide bandgap semiconductor Ga_2O_3 power diodes. *Nat Commun* **13**, 3900 (2022).
[2]- He Y, Zhao F, Huang B, Zhang T, Zhu H. A Review of β-Ga_2O_3 Power Diodes. *Materials*. 2024; 17(8):1870.

Proposed vs. Prior Art



	Current state	Proposed
Device Architecture	Lateral Devices	Vertical Devices
Breakdown Voltage	<1.5 KV	2-3 KV
Integration	2D/3D	P-type oxide or SiC
Substrate Size	Small	4’’or higher

Outcome and Impact

Cost-effective and super-efficient power devices for very high voltage and low frequency applications.