IDSPS: Integrated Power Electronics SRA –
Research, Infrastructure & Workforce Goals

Shiladri Chakraborty, IIT Bombay (Lead)

Apurv Kumar Yadav, IIT Roorkee (Co-lead)

IDSPS National Industry Consortium Conference (NICC)
Aug 30-31, 2025
New Delhi

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Indian DSPS R&D Team: Together, We Can.

Agenda

- Background and Context
- Need for Next-gen Integrated Power Electronics R&D
- Integrated Power Electronics SRA Industry Co-development Centre: Research Areas, Team, and Infrastructure Plans
- Representative Research Projects
- Workforce education programs

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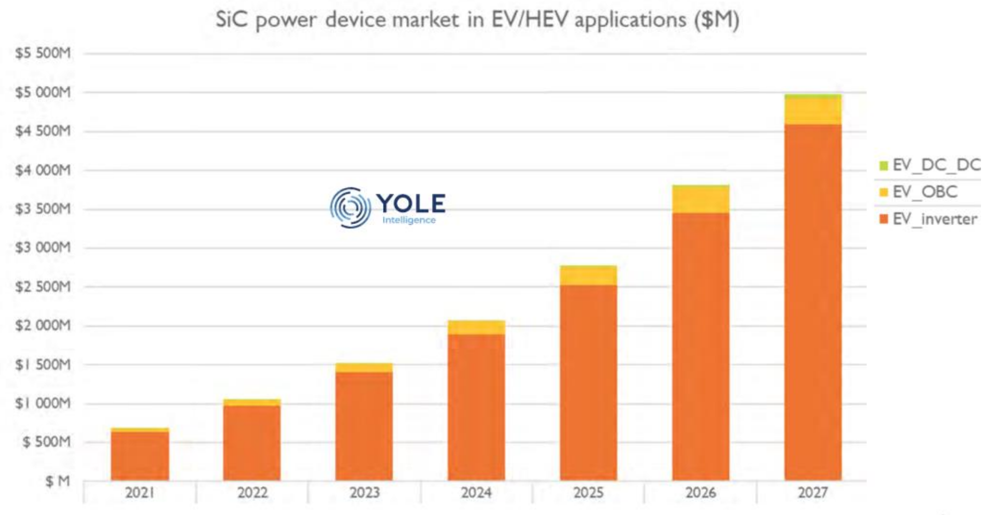
Power Electronics SRA - Financial and Technical Projections

The global power electronics market is booming

- Projected to grow from $ 61.94 billion in 2023 to $ **153.30 billion by 2030**, at a CAGR of 13.8%

Source – www.fortunebusinessinsights.com



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Major SiC market share -> Traction inverter in EVs

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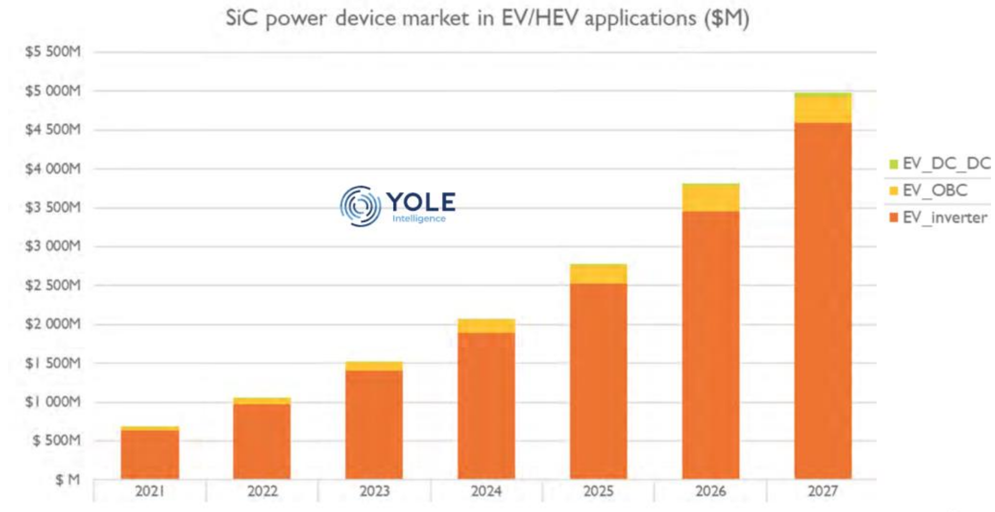

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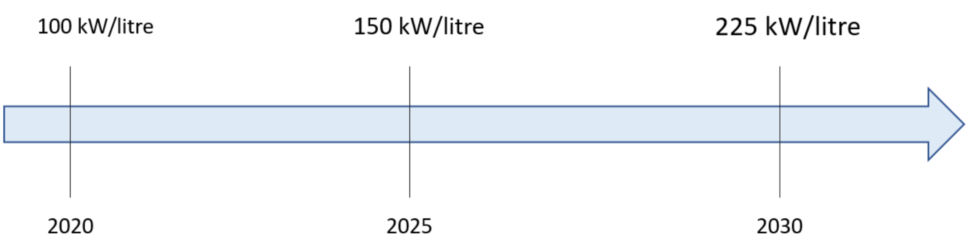
Next-gen automotive power electronics roadmap



US Department of Energy traction inverter power-density targets

(Moore's law of power electronic systems?)

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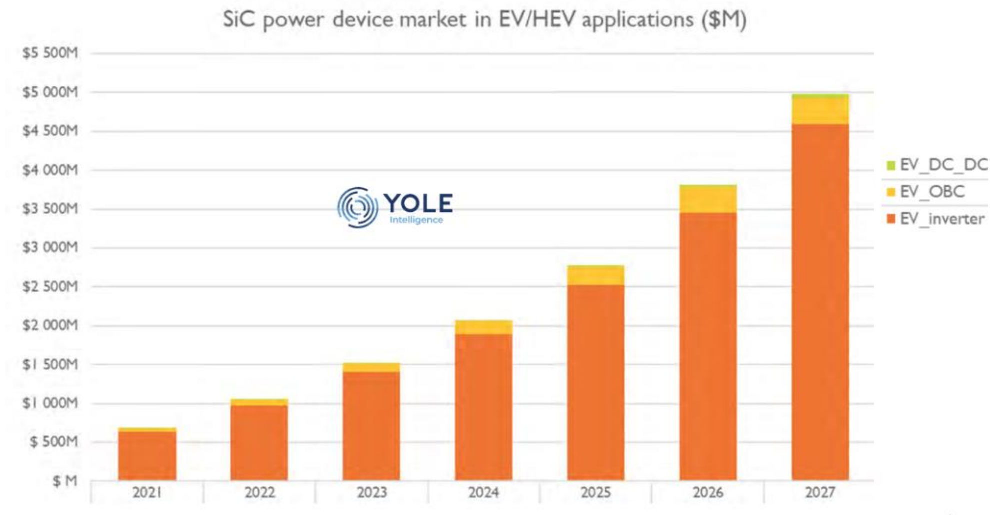

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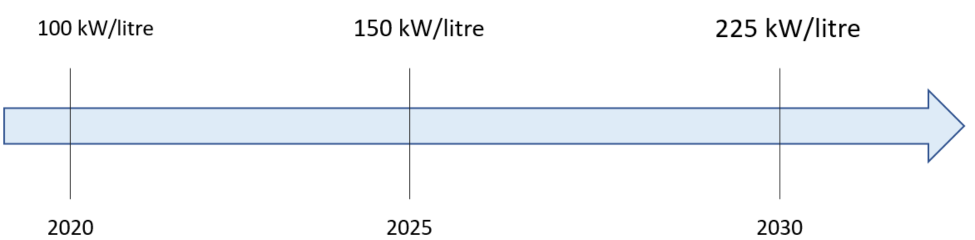

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Why efficiency/power-density matters?

- Lighter EVs with smaller battery pack, greater range
- **1 % efficiency improvement** of a 100 kW traction inverter x *1 million EVs* (driven an hr. a day) ≅ day-long **output of a 100 MW power plant!**

Power-density of current commercial inverters ≈ 10-20 kW/L

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Wide-bandgap (WBG) devices – a key enabler for next-gen power electronics

- Fundamental efficiency benefits by replacing Si with WBG

Material	Bandgap [eV]	Electron mobility μ_n [cm²/Vs]	Critical field E_c [V/cm]	Thermal conductivity [W/mK]
Si	1.12	1400	**3 x 10⁵**	130
SiC	2.36 - 3.25	300-900	**1.3-3.2 x 10⁶**	700
GaN	3.44	900; 1500-2000 (AlGaN/GaN)	**3.0-3.5 x 10⁶**	110

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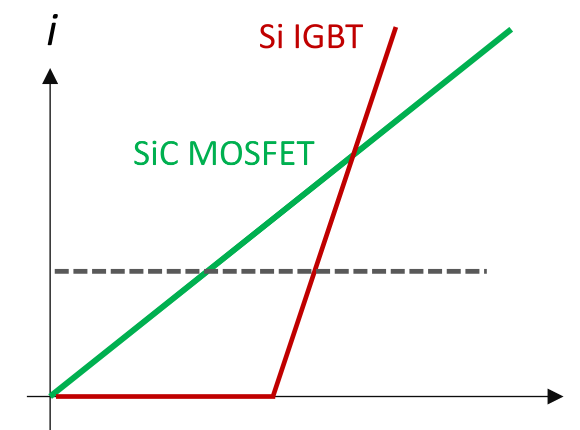
→ ***much lower conduction losses at part-load (ideal for electric cars with a start-stop mission profile)***



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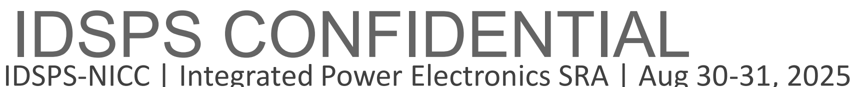
3. Higher thermal conductivity of SiC
→ ***smaller junc.- case Rth → smaller heat-sink***



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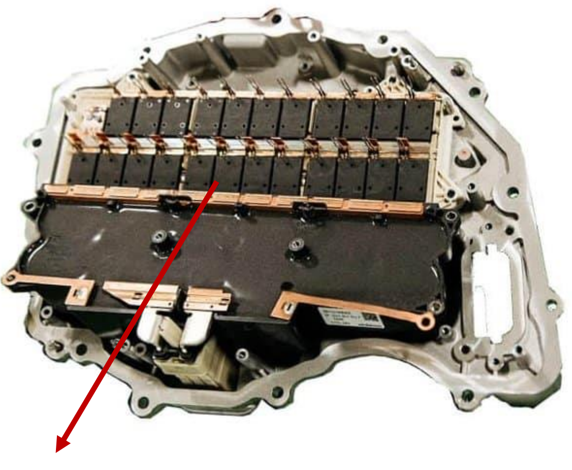
EV power electronics is migrating (…migrated?) towards WBG

Chevrolet	Volt[a]	2016	Delphi	1-in-1	12	*Si* IGBT
Tesla	Model X[e]	2016	Infineon	TO-247 discrete	84	*Si* IGBT
Toyota	Prius4G[f]	2016	Denso/Toyota	2-in-1	6	*Si* IGBT
Audi	e-Tron BEV[a]	2019	Hitachi	2-in-1	6	*Si* IGBT
Volkswagen	ID.3	2020	Infineon	6-in-1	1	*Si* IGBT
Tesla	Model 3	2018	ST Microlec.	1-in-1	24[i]	SiC MOSFET
BYD	Han[b]	2020	BYD Semicond.	6-in-1	1	SiC MOSFET
Lucid	Air	2020	[g]	[g]	[g]	SiC MOSFET

Source – Robles et. al, *"The role of power device technology in the electric vehicle powertrain,"* Wiley Energy Research, Mar. 2022.

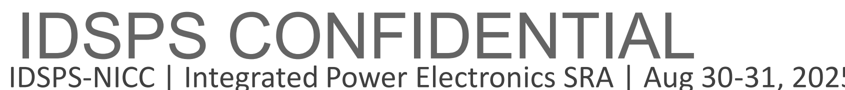
Tesla Model 3 inverter



Custom SiC power modules from ST Microelectronics (total - 24 nos.)

Source – www.pntpower.com (main source – Munro Assoc.)

Next-gen traction inverters are already adopting SiC MOSFETs instead of Si IGBTs



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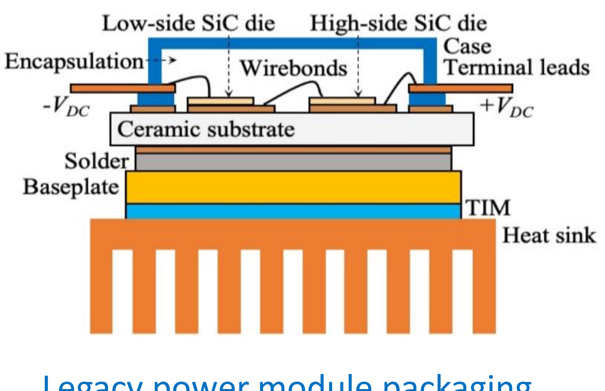
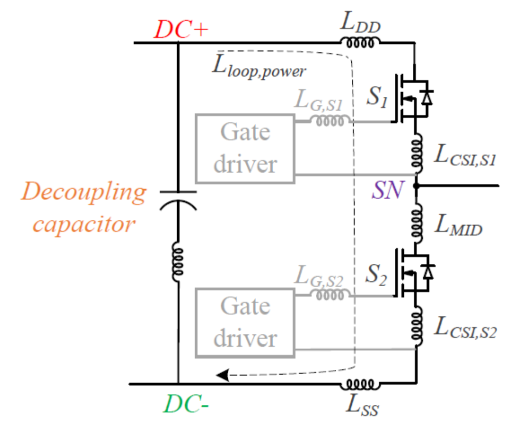
Motivation for Power Electronics Packaging R&D

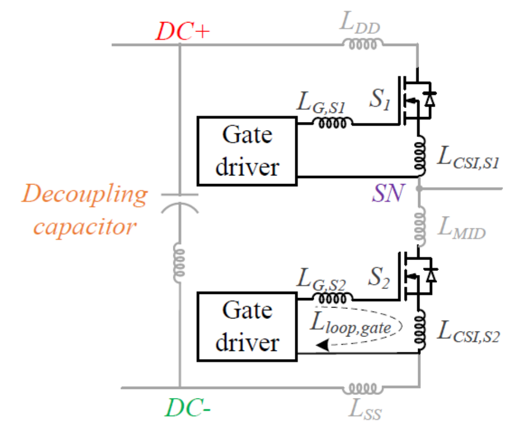
The challenge with WBG devices – legacy packaging is not enough

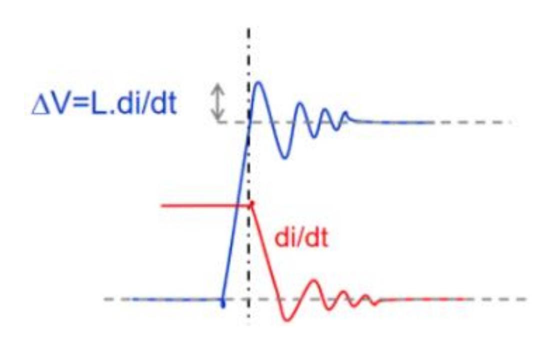
1 Electrical performance



Legacy power module packaging







Legacy packaging approach - connection of packaged power-dies with *external* decoupling capacitors, driver ICs, protection, and control circuitry - ***limits benefits of WBG devices***

- *parasitic inductances* → ***voltage spikes***
- *parasitic capacitances* (e.g. from SN to DC+/DC-) ⟶ high dv/dt of WBG devices ⟶ high common-mode currents → ***EMI and reliability concerns***

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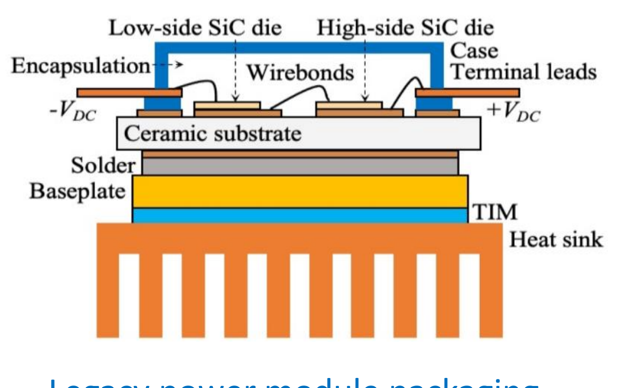

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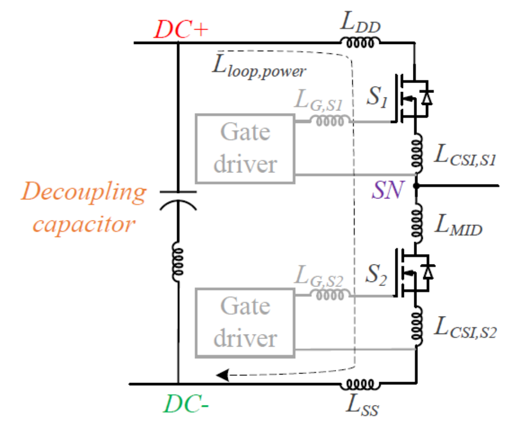

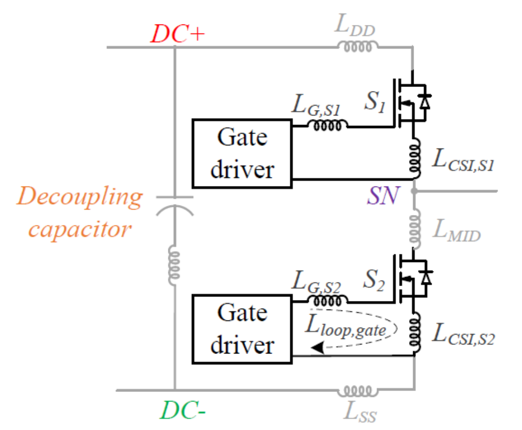

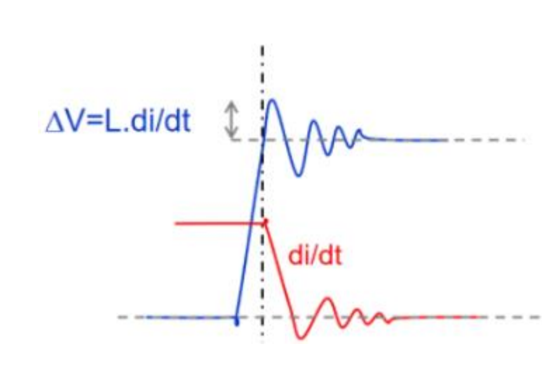

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Summary: WBG devices need packages with much lower parasitic inductance, capacitance to unleash their true potential!

Image source – www.gtspitit.com

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Motivation for Power Electronics Packaging R&D

The challenge with WBG devices – why legacy packaging is not enough

2 Thermal performance

..Not only electrical, thermal packaging must improve too!

Tesla's plan to slash silicon carbide use sends some chipmakers' shares down

PUBLISHED THU, MAR 2 2023•1:03 PM EST | UPDATED THU, MAR 2 2023•9:06 PM EST

At Tesla's 2023 Investor Day presentation on Wednesday, which largely focused on efficiency and controlling costs, powertrain engineering leader Colin Campbell took the stage to show how the company plans to reduce the cost of their cars' powertrains, while maintaining high performance and energy efficiency.

Campbell revealed that, "In our next powertrain, the silicon carbide transistors that I mentioned, that are key component[s] but expensive, we figured out a way to use 75% less without compromising the performance or the efficiency of the car."

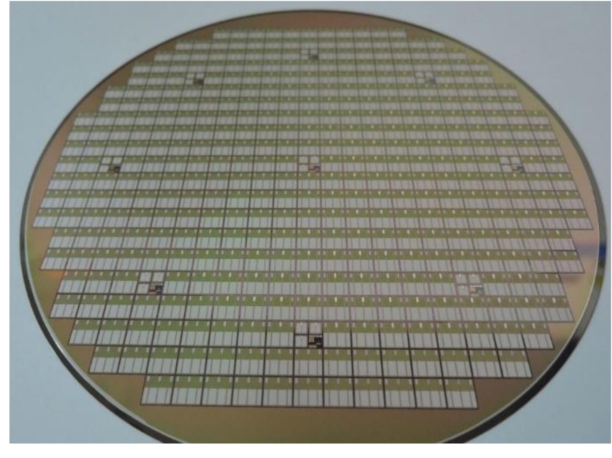


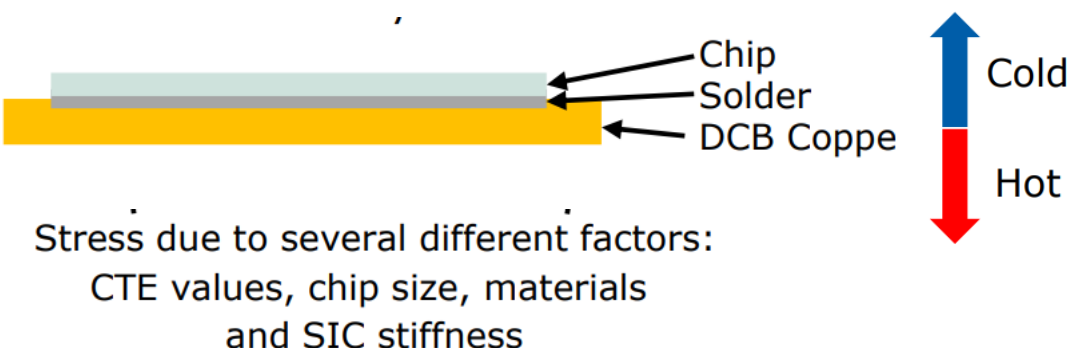
Image source – www.sumitomoelectric.com

Summary: SiC dies will get smaller
-> tougher thermal management challenge!

Motivation for Power Electronics Packaging R&D

The challenge with WBG devices – why legacy packaging is not enough

3 Reliability (thermo-mechanical) performance



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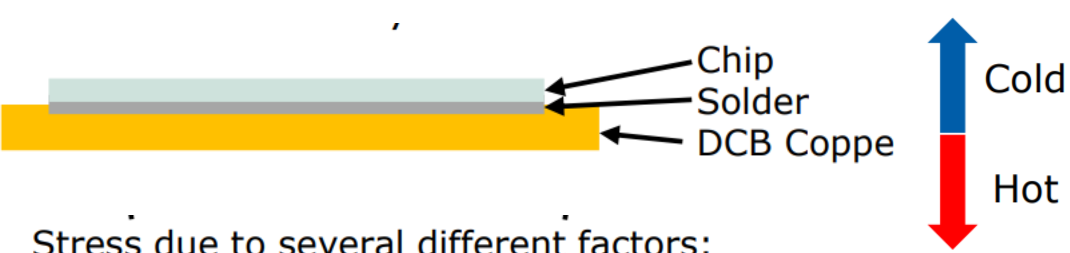

Stress due to several different factors:
CTE values, chip size, materials
and SIC stiffness

- Compared to Si, SiC has closer CTE match with solder and copper

- However, the extremely high Young's Modulus of SiC means that despite closer CTE Match, SiC dies are subjected to greater thermo-mechanical stress

	Coefficient of Thermal Expansion (CTE) [10^{-6}/^{o}C]	Young's Modulus [Gpa]
Si	2.6	62
SiC	4	**450**
Solder	23	40
Copper	17	117

Courtesy David Levett, *Power America webinar*.

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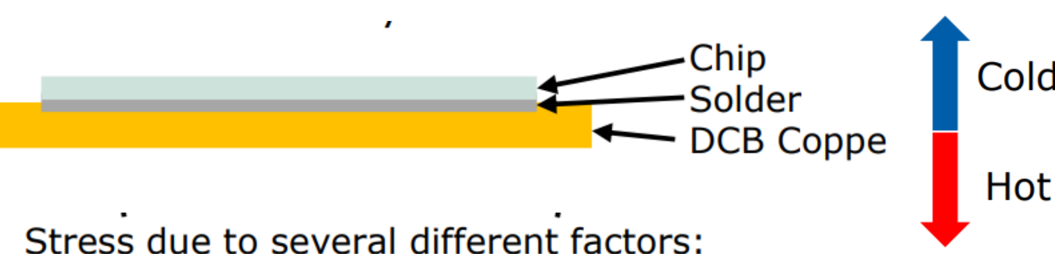

Stress due to several different factors:
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Summary: SiC dies can exhibit worse thermal cycling behaviour than Si counterparts

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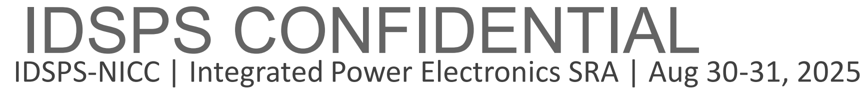
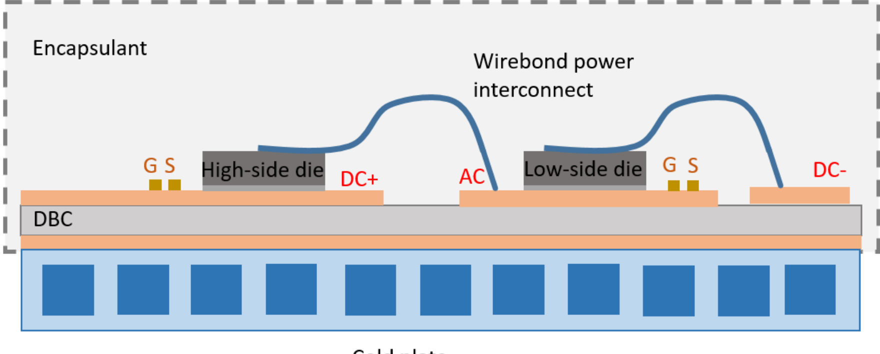


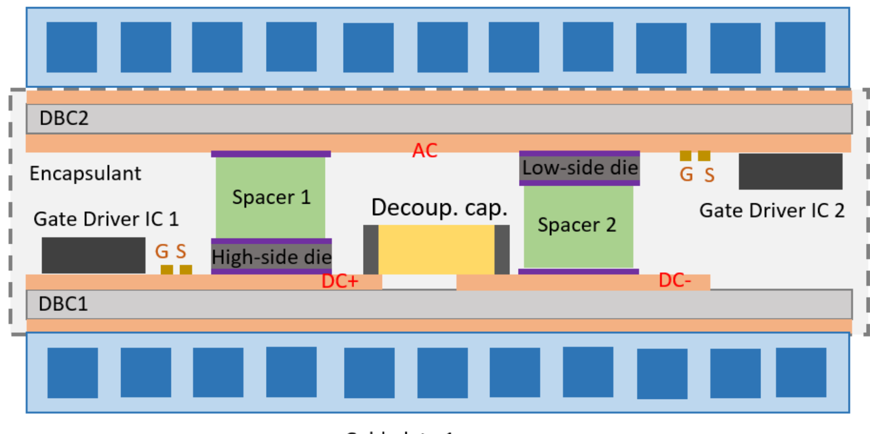
Motivation for Power Electronics Packaging R&D

Alternate design architectures can address the challenges

(*Prior Art*) - **Single-side-cooled, wire-bonded, soldered, 2D**



(*Future*) - **Double-side-cooled, wire-bondless, heterogeneously-integrated, sintered, 3D**



Advantages of 3D architecture

- Lower loop areas, heterogeneous integration → lower inductances → ***faster, efficient switching***
- Double-sided heat extraction → lower thermal resistance → ***smaller heat-sink***
- ***No power wire-bond-related failures***
- Sintering → ***better thermo-mechanical reliability,*** lower contact resistance → ***better thermals***

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Research Vision: Strategic Research Focus Areas

All parts of the "eco-system" need innovations

⑥ Sintered interconnect

⑦ Substrate

Cold plate 2

⑧ Gate Driver

⑤ Encapsulant

DBC2

AC

G S

G S

⑨ Sensing & Testing

④ Spacer

DC+

DC-

DBC1

① Architecture, Design, Assembly

Power die 1
(high-side)

② Cold plate 1

Power die 2
(low-side)

③ Decoupling capacitor

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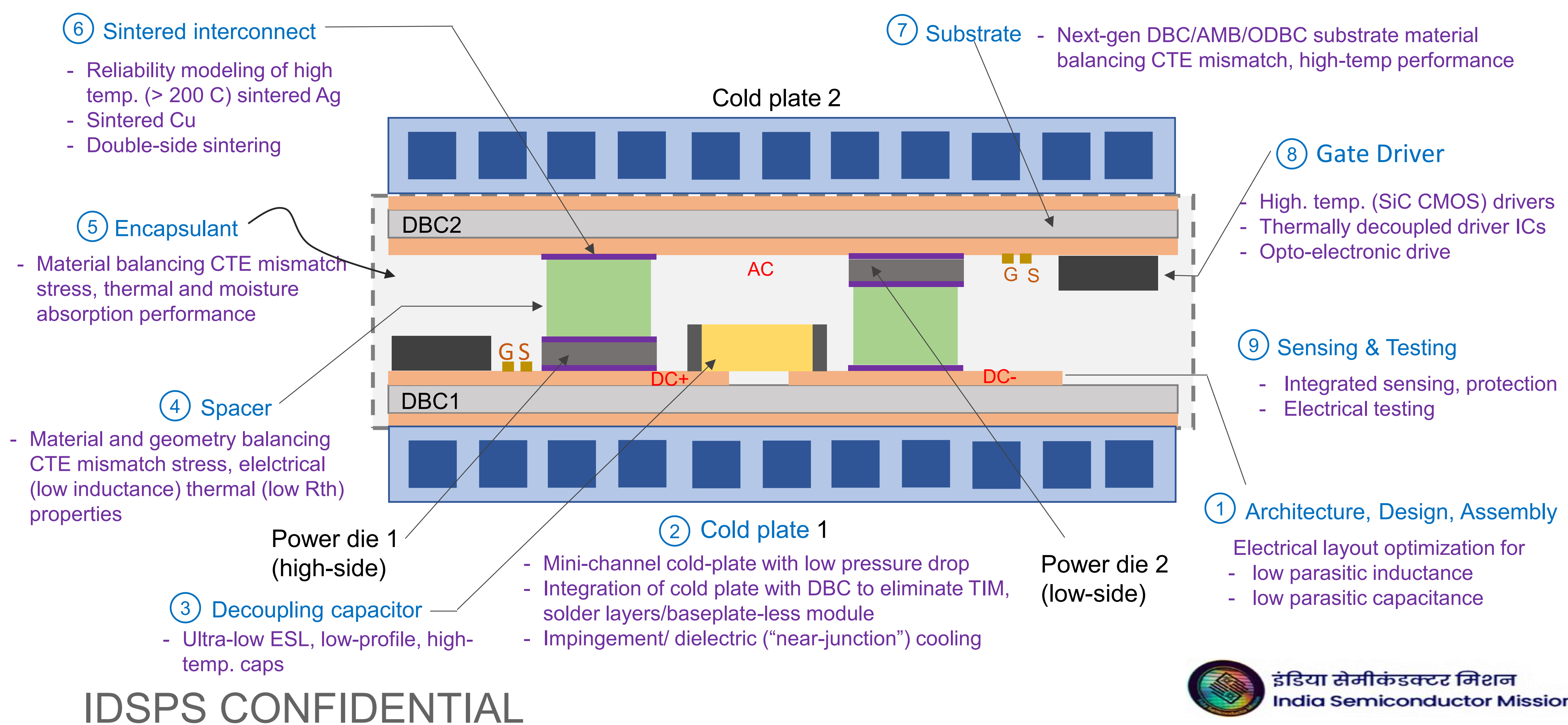

Research Vision: Strategic Research Focus Areas

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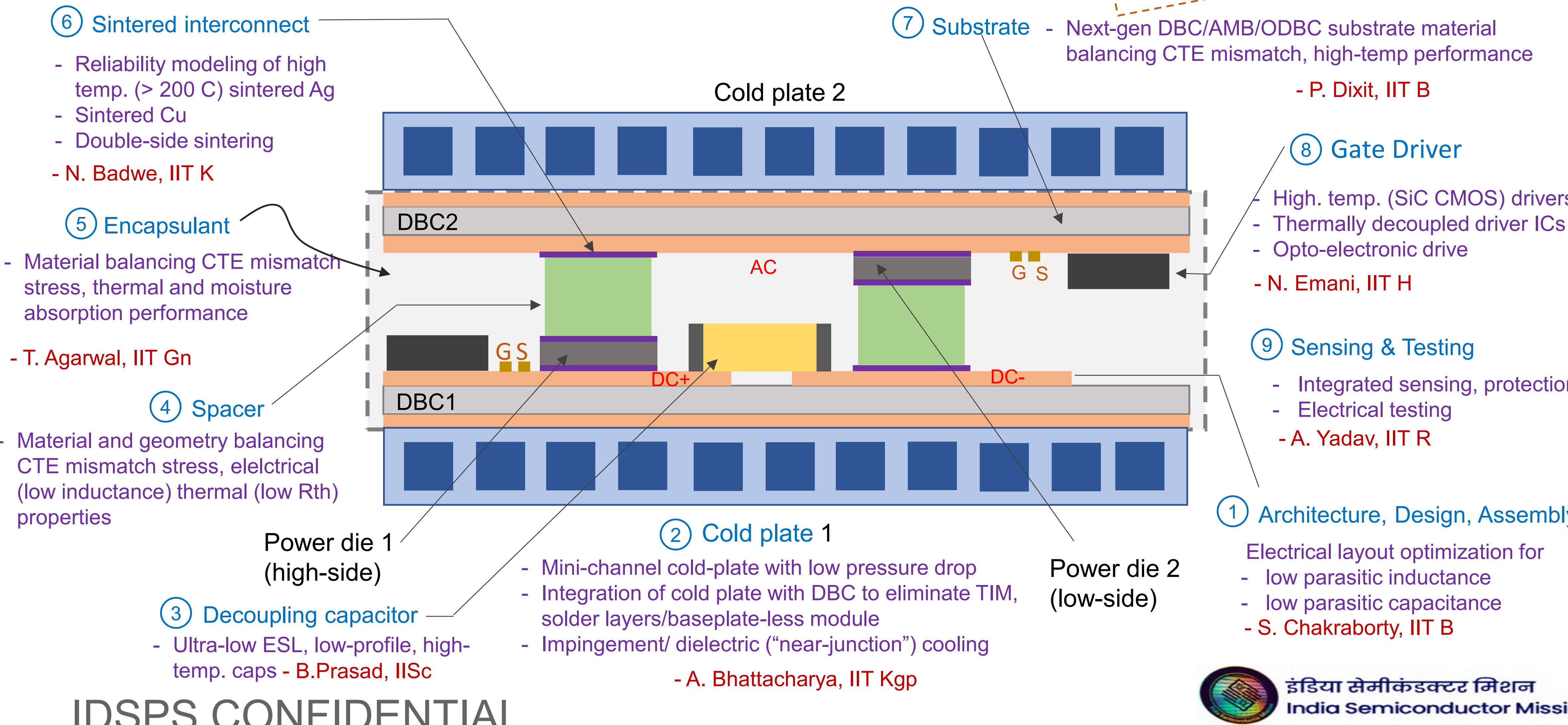
"System-level" cross-disciplinary focus - A key distinguishing feature of the IDSPS program



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Multidisciplinary India-wide Faculty Team with Expertise in Strategic Areas

Core Faculty Team

Shiladri Chakraborty
(EE, IIT B) - **Lead**
Power electronics, SiC pkgng.

Soumya Shubhra Nag
(EE, IIT D)
Power electronics, PCB-embed. pkgng.

Apurv Kumar Yadav
(EE, IIT R) - Co-lead
Power electronics, motor drives

Pradyumn Chaturvedi
(EE, VNIT Nagpur)
Power electronics, solid-state-transf.

Saptarshi Basak
(EE, IIT D)
Motor drives, electrical machines

....

Cross-SRA Faculty with relevant expertise

Anandaroop Bhattacharya
(ME, IIT Kgp)
Thermal management

Pradeep Dixit
(ME, IIT B)
Substrates

Nilesh Badwe & Shiv Govind Singh
(MsE, IIT K) & (EE, IIT H)
Interconnects, die-attach

Ankush Bag
(EE, IIT G)
GaN power devices

Bhagwati Prasad
(MsE, IISc)
Materials

Tarun Agarwal
(EE, IIT Gn)
Pred. modeling, reliability

Naresh Emani
(EE, IIT H)
Optoelectronic drive

Parlapalli V Satyam & Akshay K
(EE, IIT Bhub.)
SiC power devices

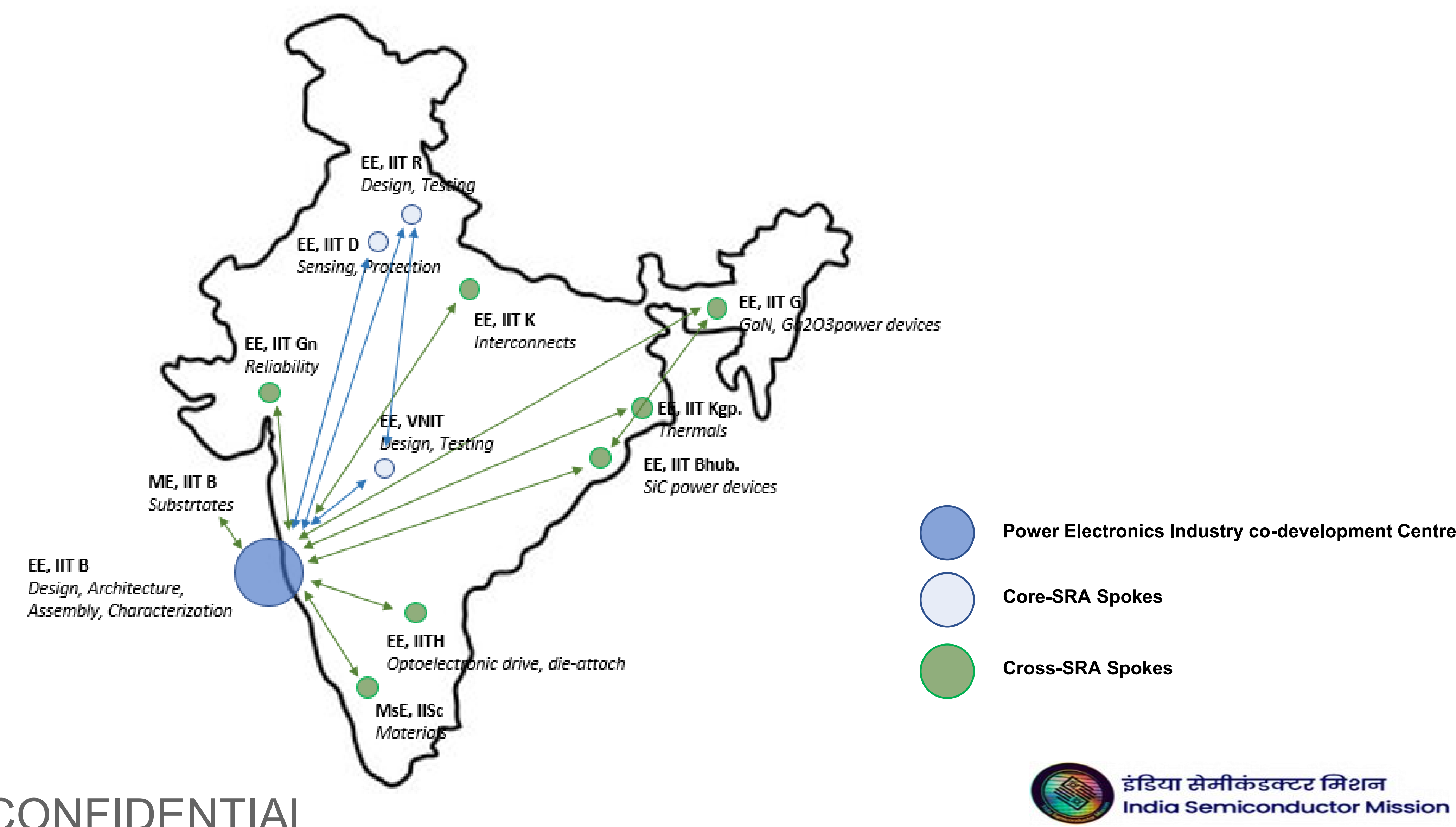
....

Global Academic Collaborators

Alan Mantooth
(EE, Univ. of Arkansas)
2D/3D power packaging, heterogeneous integration, SiC CMOS gate drivers

Vanessa Smet
(EE, Georgia Tech.)
Multi-physics packaging, thermal management, die-attach

Hub and Spoke Structure for R&D and Workforce Education



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Proposed ICC: State-of-the-art Infrastructure Facilities with Process Flow

1. Design Lab

- *Layout, simulation, design* PC workstations with design softwares (2 Cr)

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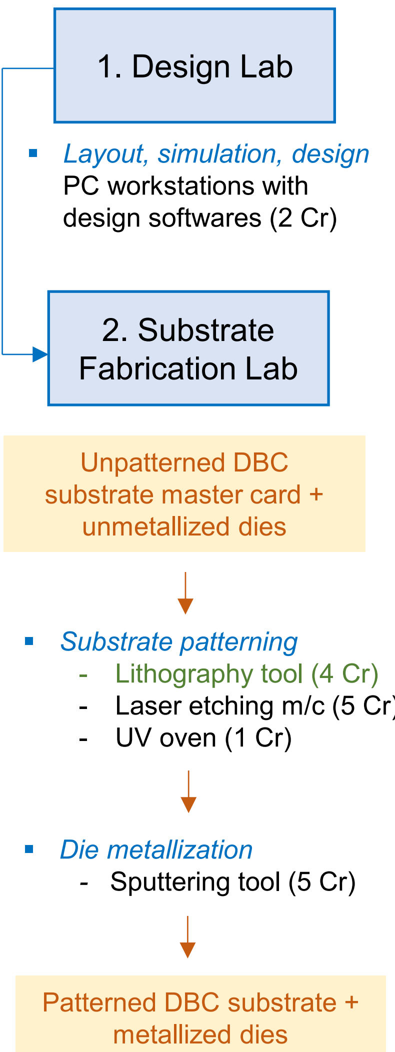

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  PC workstations with design softwares (2 Cr)

2. Substrate Fabrication Lab

Unpatterned DBC substrate master card + unmetallized dies

↓

- *Substrate patterning*
  - Lithography tool (4 Cr)
  - Laser etching m/c (5 Cr)
  - UV oven (1 Cr)

↓

- *Die metallization*
  - Sputtering tool (5 Cr)

↓

Patterned DBC substrate + metallized dies

3. Assembly Lab

Patterned DBC substrate + metallized dies

↓

- *Pre-cleaning*
  - Low-pressure plasma cleaner (2.5 Cr)

↓

- *Ag-sintering of die*
  - Precision die bonder (7.5 Cr)

↓

- *Soldering of spacers, caps, ICs*
  - Screen printer (0.5 Cr)
  - Solder vacuum oven (5 Cr)
  - Brazing furnace (5 Cr)

↓

- *Wire-bonding*
  - Heavy wire bonder (0.75 Cr)
  - Wedge bonder (0.75 Cr)

→

- *Optical inspection*
  - Digital micrometer (2 Cr)

↓

- *Void-free encapsulation*
  - Dispensing vacuum chamber (2 Cr)

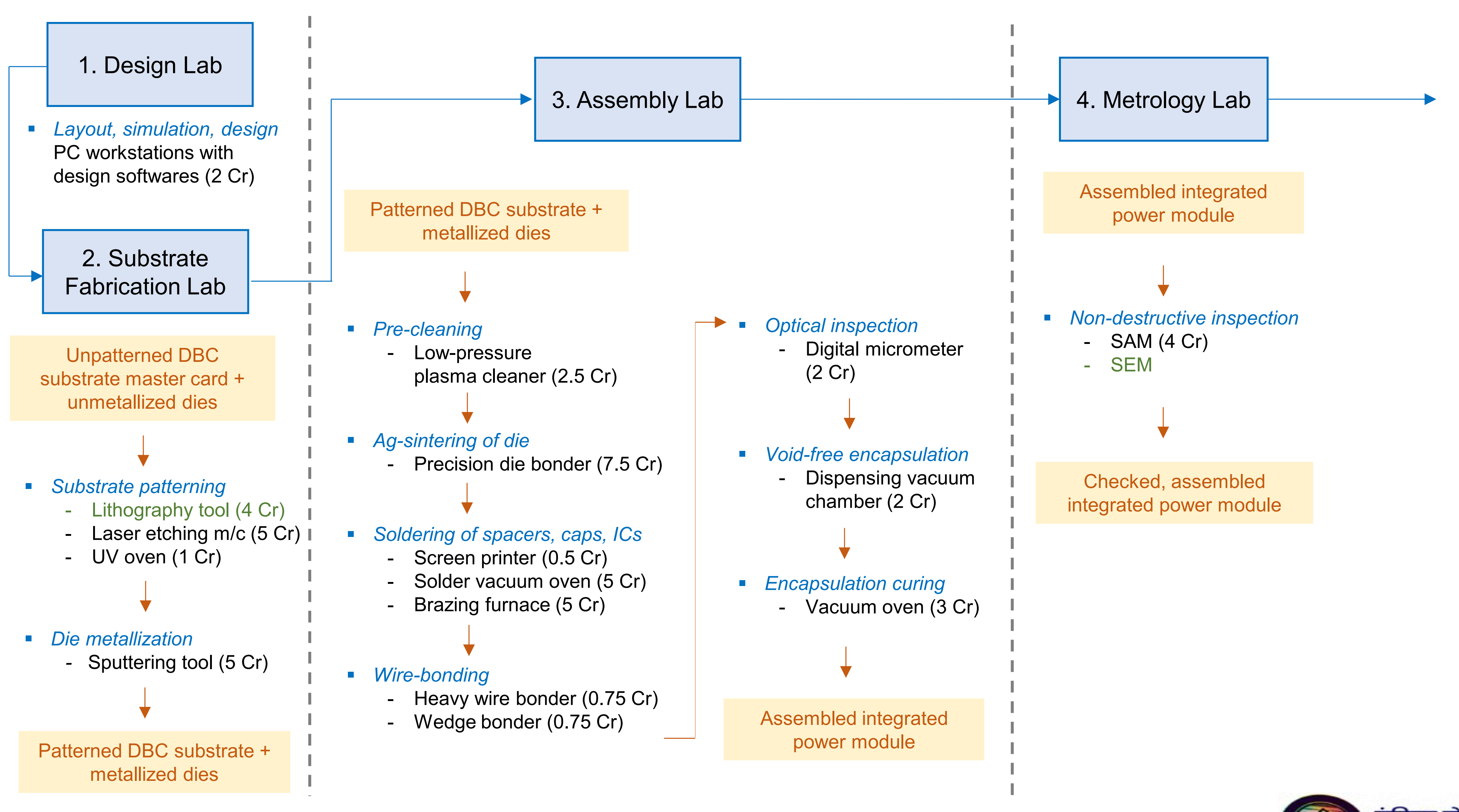
↓

- *Encapsulation curing*
  - Vacuum oven (3 Cr)

↓

Assembled integrated power module

Proposed ICC: State-of-the-art Infrastructure Facilities with Process Flow



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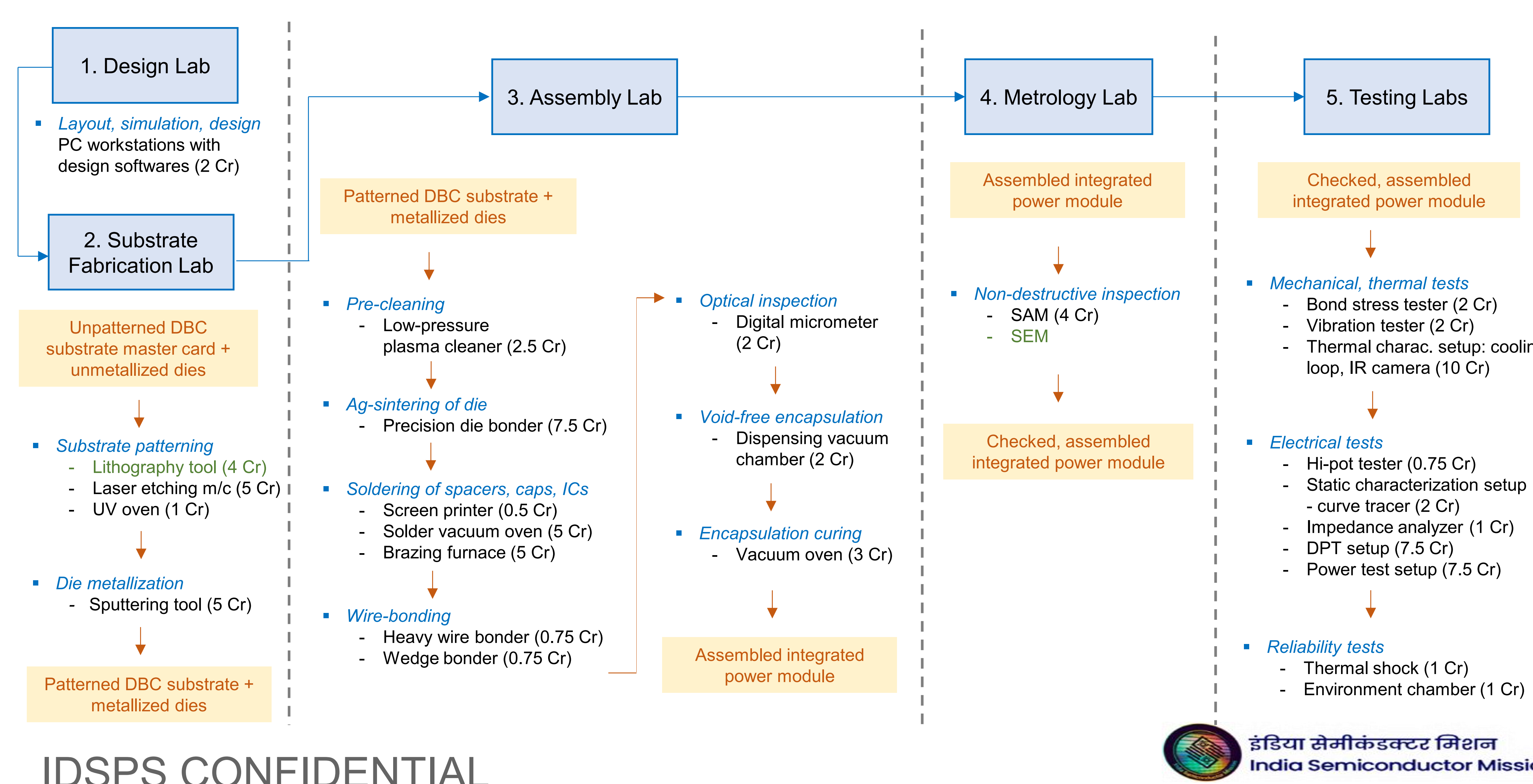
Proposed ICC: State-of-the-art Infrastructure Facilities with Process Flow



Global Industry Partners

Currently interested industry partners

- MacDermid Alpha
- Texas Instruments
- Delta Electronics
- CDIL
- Ansys
- John Deere
- RIR Power Electronics

Potential future industry partners

- Tata Motors
- Reliance
- Wolfspeed
- Infineon
- On Semi
- ST Micro
- Renesas
- AT&S
- Tata Electronics
- ROHM
- Henkel
- Semikron
- Vishay
- Fuji
- Mitsubishi Electric
- Toshiba
- NXP Semi
- Micro Semi
- Rogers
- Kyocera
- TDK
- Danfoss
- Dupont
- Resonac
- Bosch
- Denka
- Semicosil

….

Industry type	Example research areas of interest
• OEM	High power-density traction inverter, charger design
• Tier 1 Supplier	High power-density traction inverter, charger design
• Component Supplier	Novel integrated power module architectures
• Materials Supplier	High-temperature capacitors, novel TIM, Cu-sintering material, next-gen substrates
• Design	Fast design optimization software tools

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Agenda

- Background and Context
- Need for Next-gen Integrated Power Electronics R&D
- Integrated Power Electronics SRA Industry Co-development Centre: Research Areas, Team, and Infrastructure Plans
- Representative Research Projects
- Workforce education programs

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Updated List of R&D projects

- ***Category 1 - SiC/Si (vertical device) integrated module design***

1. Design and architecture of next-gen, 3D integrated power modules (Chakraborty Et al.)
2. Predictive modeling and design for thermo-mechanical reliability enhancement of 3D, DSC, sintered power modules (Chakraborty Et al.)
3. Fabrication and testing of 3D, DSC, heterogeneously-integrated, sintered power modules (Chakraborty Et al.)
4. Design and architecture of 3D, DSC package for multi-phase, four-quadrant MOSFETs for next-gen matrix converters (Chakraborty Et al.)
5. 1200 V, 40 A SiC 3-Level T-NPC Power Module for EV Chargers (Nag)

- ***Category 2 - GaN (lateral device) integrated module design***

6. GaN based power module with series connected GaN devices for high-voltage applications (Yadav Et al.)
7. GaN-SiC hybrid full bridge module for EV applications with integrated sensing and ultrafast protection (Nag)
8. GaN based 3-Level half-bridge power module for low-voltage high-current traction Inverter (Yadav)
9. PCB-DBC hybrid multi-chip GaN power module for high-current applications (Chakraborty Et al.)
10. 150 V, 260 A GaN Half-Bridge Power Module for Light Electric Vehicles (Nag)

- ***Category 3 - Application-oriented***

11. Ultra-high-efficiency, reliable, and high-power-density solid-state transformer (Chaturvedi Et al.)
12. Impact of Thermal Packaging on the Performance of EV Motor Drives (Basak)
13. Matrix-based compact 22 kW, 800 EV, 3-ph. OBC employing multi-phase-integrated GaN BDS and integrated planar magnetics (Chakraborty Et al.)
14. GaN-based ultra-high efficiency (99.5 %), sub-kW, 1-ph, wide input range (universal-input) PFC (Chakraborty Et al.)
15. 48-12 V, 6 kW, ultra-compact (quarter-brick), ultra-high-efficiency (99.5 %) DC-DC converter for data centers employing modular GaN cells and integrated planar magnetics (Chakraborty Et al.)

Green – New projects (added after ISPEC 2025)

Details of Representative Projects

Project 1 - Design and architecture of next-gen, 3D integrated power modules

Team: **Shiladri Chakraborty (EE, IITB)**, Pradeep Dixit (ME, IITB), Nilesh Badwe (MSE, IITK), Alan Mantooth (Univ. of Arkansas)

Objective:

- Explore diff. 3D architectures for DSC, wire-bondless, *multi-chip (high-current)* SiC half-bridge module with *integrated capacitor*
- *Balance and minimize* power loop and gate *loop inductances*

Outcome:

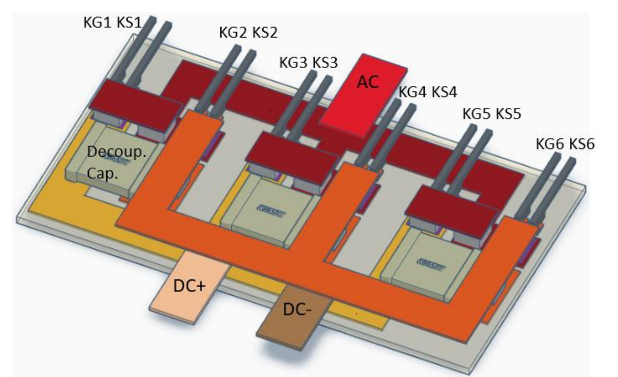
Optimized design of 3D, DSC, multi-chip SiC module for high-current traction inverters.

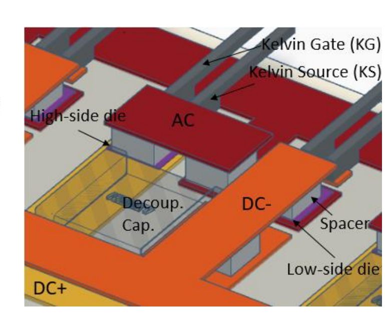
Proposed vs. Prior Art:

Parameter	Current Status	Proposed
Architecture	2D-multi-chip, SSC with wire-bonds/ 3D-single-chip, DSC without wire-bonds [1], [2]	3D-multi-chip, DSC without wire-bonds
Diff. in PLI of parallel loops	<1.9 nH for 2D-multi-chip	< 0.1 nH
Terminations	AC and DC terminals on same side/DC+ and DC- on opposite sides; unsuitable for system integration of phases	DC terminals on same side, AC on opposite side; suitable for system integration of multiple phases

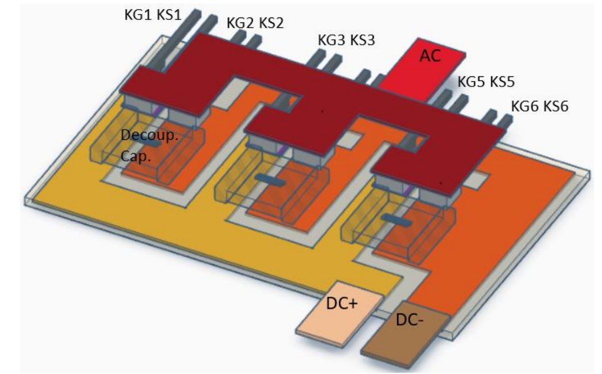
[1] Ding et al., "*A Double-Side Cooled SiC MOSFET Power Module With Sintered-Silver Interposers*," TPEL, Oct. 2021.
[2] R. Paul et al., "*A Double-sided Cooled Power Module with Embedded Decoupling Capacitors*," JESTPE, Early Access.

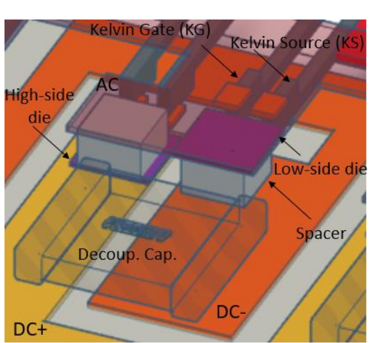
Approach:





Design architecture 1





Design architecture 2

Project 2 - Predictive modeling and design for thermo-mechanical reliability enhancement of 3D, double-side-cooled, sintered power modules

Team: **Tarun Agarwal (EE, IITGN)**, Shiladri Chakraborty (EE, IITB), Nilesh Badwe (MSE, IITK), Anandaroop Bhattacharya (ME, IITKgp)

Objective: Explore *design strategies of encapsulant and spacers* for *addressing CTE-reliability challenges* of 3D, double-side-cooled (DSC), sintered power modules, while *balancing electrical, thermal, and moisture ingress performance*.

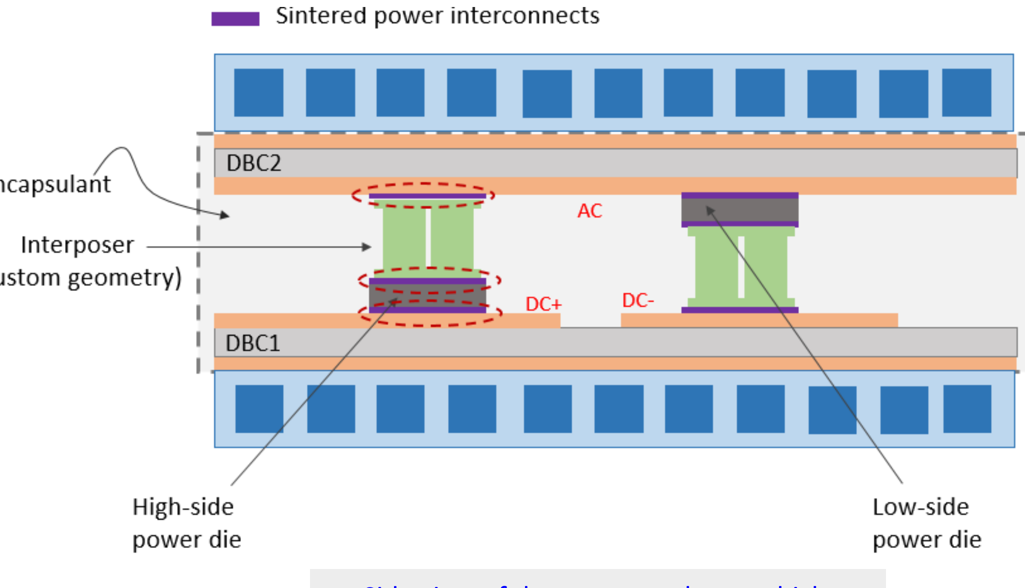
Outcome:

Predictive modeling framework enabling design of *industry-grade 3D, DSC modules* with low CTE stress at the three interfaces.

Proposed vs. Prior Art:

Parameter	Current Status	Proposed
Encapsulant	Silicone gel	Variety of encapsulants including high-modulus ones
Bonding interface	Soldering/Ag-sintering	Soldering/Ag-sintering
Interposer geometry	Solid block, trenched, octagonal, X-shaped, trapezoidal	Custom geometries
Moisture absorption	Not considered	Considered

Approach:



Side view of the conceptual test vehicle

- *Impact of encapsulants (having different CTE, modulus)* on the bonding interfaces
- *Interposers with different shapes and dimensions*
- *Simulation to quantify stress* (e.g., strain energy density/cycle) and develop *theoretical reduced order models*

[3] X. Cao et al., "*Planar power module with low thermal impedance and low thermomechanical stress*," TCP. Aug. 2012.
[4] JF. Boshkovski et al.,"*Effects of Encapsulant Properties on the Thermo-Mechanical Reliability of DSC Power Modules for Traction Inverters*," ECCE 2023.

Project 4 - GaN-based power module with series-connected GaN devices for high-voltage applications

Team: **Apurv Kumar Yadav (EE, IITR)**, Shiladri Chakraborty (EE, IITB), S G Singh (EE, IITH), A Bhattacharya (ME, IITKgp)

Objective: Develop HV half-bridge module having *multiple series-connected GaN devices* that can *dynamically balance voltages* across the devices by *active control of gate current*, with minimal voltage overshoot.

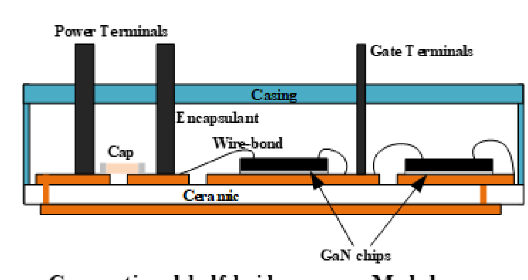
Outcome:

- Board-level design validating the proposed active gate driving
- Heterogeneous integration of power devices with active gate driving circuit
- Development of hardware prototype having 1200 V withstanding capability

Proposed vs. Prior Art:

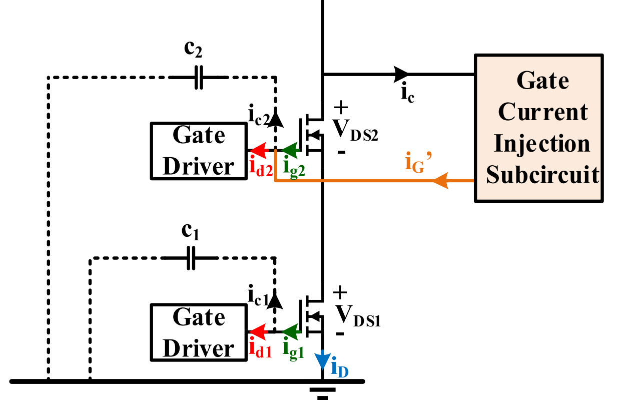
Parameter	Current Status	Proposed
Blocking Voltage	650 V [5]	~ 1200 V
Transient Voltage	750 V [5]	~ 1400 V
Maximum tolerable delay	30 ns Si IGBT, 20ns SiC [5]	~15 ns GaN
Series connection of GaN	Iterative method [6]	Online method with fast responsive active gate driving
Series connection of devices	Si IGBTs, SiC [6]	GaN
GaN Power Module integration	Half and full bridge [5]	Series-connected GaN devices with integrated active gate driver

Approach:



Conventional half-bridge power Module

Proposed series connected GaN power module



Active gate driver for series connected GaN devices

[5] B. Passmore et al., *"A 650 V/150 A enhancement mode GaN-based half-bridge power module for high frequency power conversion systems,"* ECCE 2015.
[6] A. I. Emon et al.,*"Design and optimization of 650 V/60 A double-sided cooled multichip GaN module,"* APEC 2021.

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Project 5 - Ultra-high-efficiency, reliable and high-power-density solid-state transformer

Team: **Pradyumn Chaturvedi (EE, VNIT)**, Mohd. Alam (EE, VNIT), Shiladri Chakraborty (EE, IITB)

Objective: Design and *development of SST with optimized magnetics, reconfigurable & modular structure and embedded components* for various applications including fast EV charging, future smart DC grid, aerospace, defense, data centers etc.

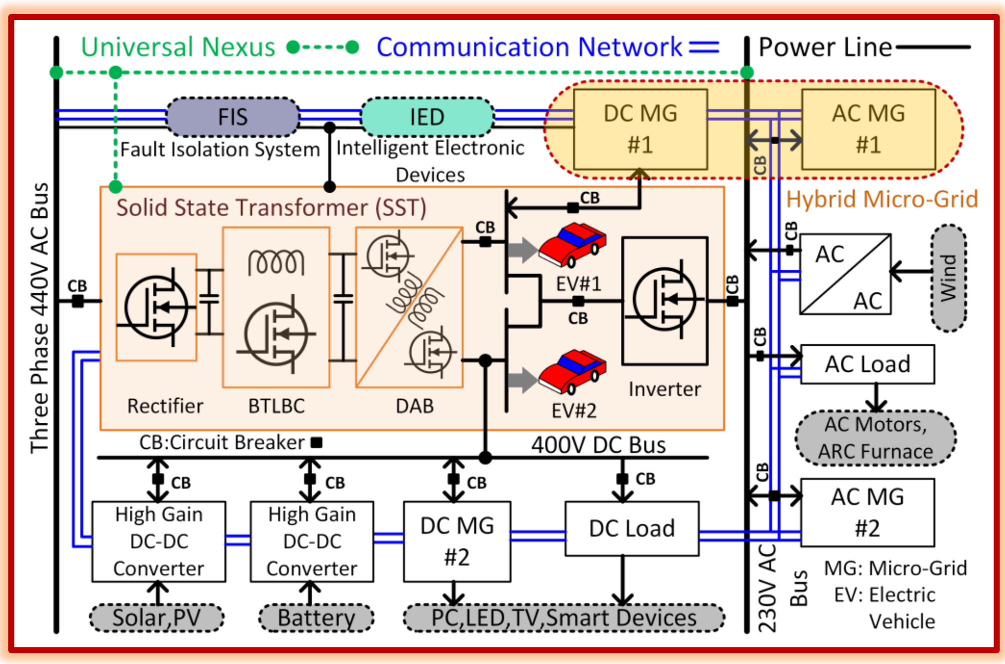
Technical Challenges:

Optimized structure design, optimized control of various SST components, protection, safety, thermal management, cost etc.

Main features as per modern industry need:

- High power-density, excellent thermal management, high efficiency
- Excellent reliability, protection and safety features
- Bidirectional control of active and reactive power
- Ease of integration of various RES, EVs and other sources/loads
- Inherently improved electrical power quality
- Ease of interface with communication system and IOT devices etc.

Approach:



System-level block diagram of future power grid with SST

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Project 6 - GaN-SiC hybrid full bridge module for EV applications with integrated sensing and ultrafast protection

Team: **Soumya Shubhra Nag (IITD)** and Sumit Kumar Pramanick (IITD)

Objective: Integrate *PCB-embedded high-bandwidth current sensing* in GaN full-bridge (B6 structure) and *GaN-SiC hybrid full-bridge* (B4 structure) power modules for *ultrafast over current protection.*

Outcome:

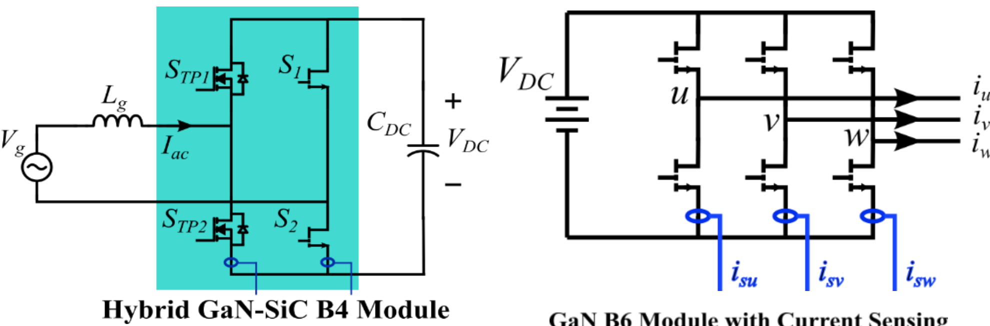
Reliable and ready-to-integrate GaN+SiC B4 & GaN B6 modules for automotive industry, e.g., 2w/3w/4w charger, BLDC drive, etc.

Proposed vs. Prior Art:

Parameter	Current Status	Proposed
Hybrid GaN+SiC Module	Not commercially available	650 V, 40 A hybrid GaN+SiC B4 module
GaN HEMT B6 module with embedded current sensing	Not commercially available	650 V, 40 A GaN B6 module with lossless, high-BW current sensing
Rogowski Coil (RC) based embedded current sensor	No commercial product available	50 mV/A, 400 MHz RC current sensor
Rogowski Coil (RC) based over-current protection circuit	No commercial product available	Sub 50 ns over-current fault protection

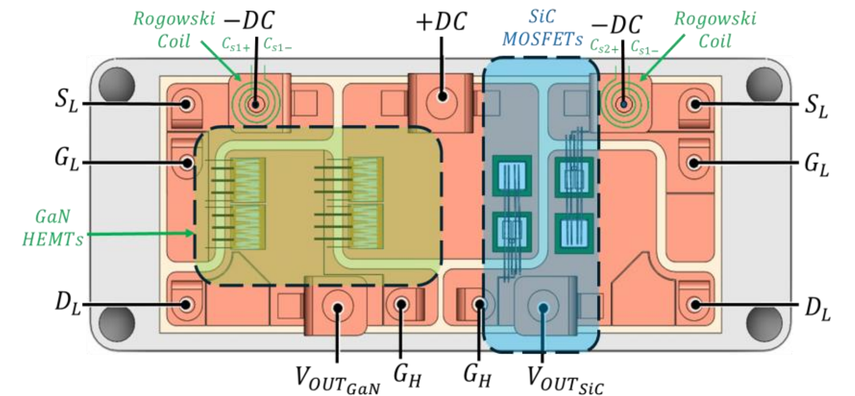
[9] Jiang et al., *"An Integrated GaN Overcurrent Protection Circuit for Power HEMTs Using Sense HEMT,"* TPEL , Aug.. 2022.
[10] Rafiq and Pramanick.,*"Ultrafast Protection of Discrete SiC MOSFETs With PCB Coil-Based Current Sensors,"* TPEL , Feb. 2023.

Approach:



GaN-SiC B4 for Totem Pole PFC

GaN B6 for BLDC inverter



Top view of GaN-SiC module with integrated Rogowski current sensor

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Project 8 - GaN based 3-Level Half-bridge Power Module for Low Voltage High Current Traction Inverter

Team: **Apurv Kumar Yadav (EE, IITR)**

Objective: Develop a GaN-based 3-level half bridge power module with reduced stray inductance for low-voltage and high-current traction inverter.

Outcome:

- Heterogeneous integration of pre-packaged low voltage and high current top-cooled GaN dies.
- Use of bottom DBC for thermal management and top double-layer re-distribution layer for interconnections with low stray inductances.
- Solderable terminals for power and signal for easy mounting of PCB mounting with direct mounting to heat sink

Approach:

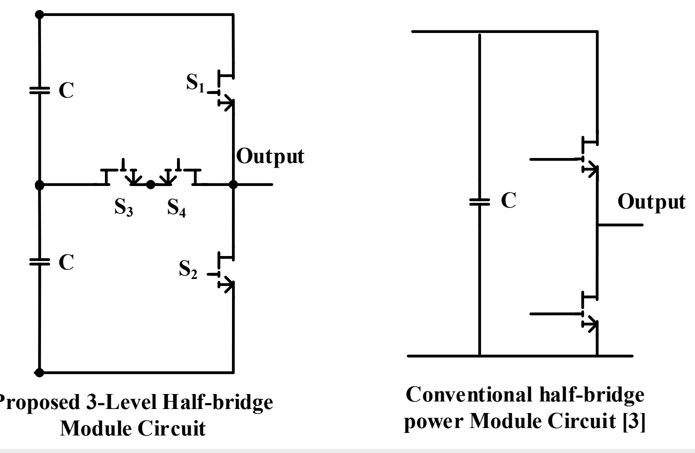
Power Terminals
Gate Terminals
Casing
Encapsulant
Wire-bond
Cap
Ceramic
GaN chips

Conventional half-bridge power Module

Encapsulation
Power Terminals
Gate Terminals
Cap
Cap
Re-distribution layer
Ceramic
Vias
GaN Devices
Die attach
DBC
TIM
Thermal interface

Proposed 3-level half bridge GaN power module

Cross-section of modules



Proposed 3-Level Half-bridge Module Circuit

Conventional half-bridge power Module Circuit [3]

Converter circuit for GaN based power modules

Proposed vs. Prior Art:

Parameter	Current Status	Proposed
Device Used	Si IGBTs, SiC	~ GaN
On state resistance	22.5 mΩ for SiC [15]	~ 5 mΩ
Input capacitance	6.6 nF for SiC [15] and 25 nF for Si IGBT	~3.1 nF
Reverse transfer capacitance	0.02nF for SiC [15]	0.02 nF
Stray inductance	>10nH [16]	< 2nH
GaN Power Module integration	Half and full bridge [16]	3-level bidirectional switch

[15] Microchip Three Level Inverter SiC MOSFET Power Module MSCSM170TLM23C3AG
[16] A. I. Emon et al., "*A Review of High-Speed GaN Power Modules: State of the Art, Challenges, and Solutions,*" JESTPE, June 2023.

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Indian DSPS R&D Team: Together, We Can.

Agenda

- Background and Context
- Need for Next-gen Integrated Power Electronics R&D
- Integrated Power Electronics SRA Industry Co-development Centre: Research Areas, Team, and Infrastructure Plans
- Representative Research Projects
- Workforce education programs

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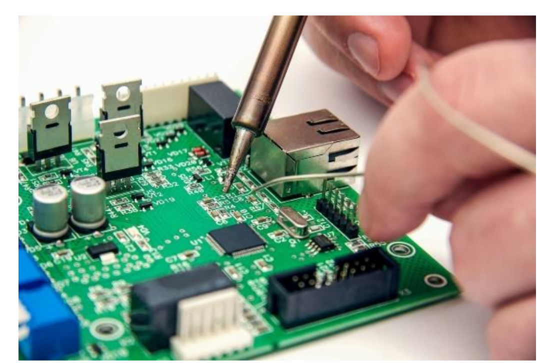
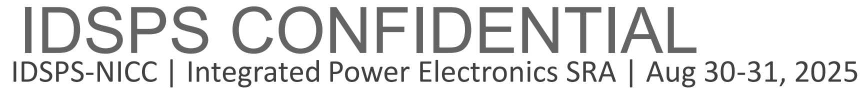
Current Skill Gaps and Challenges

- **Identified Skill Gaps**
  - Knowledge in *wide bandgap (WBG) semiconductors* (SiC, GaN).
  - Proficiency in *simulation tools*, *device design*, *application circuits*, *thermal management*, and *reliability testing*.

- **Challenges in Workforce Development**
  - Rapidly evolving technology vs. slow curriculum updates.
  - Limited exposure to hands-on industry practices.
  - Need for interdisciplinary expertise in semiconductor physics, circuits, magnetics, mechanical engineering, and control systems.





IDSPS Technology Workforce education programs

- **Short-term:**
  - Identify course curriculum needs - Done
  - Develop graduate-level theory course on WBG power devices, systems, and packaging – In Progress
  - Knowledge acquisition: webinars, in-person expert workshops - Done

IDSPS Technology Workforce education programs

- **Short-term:**

Professional Development Course (PDC)

INTRODUCTION TO DEVICE AND SYSTEMS PACKAGING

September 21st – November 30th 2024

As India begins its long-awaited journey in semiconductors and packaging, India needs to acquire the state-of-the-art knowledge to bring itself to global level. Integrated systems packaging is becoming more valuable than either semiconductors or packaging as Moore's Law benefits slow down.

This course is based on **integrated semiconductors and packaging R&D** and the textbook by **Prof. Rao Tummala and his Georgia Tech Team in the USA - Fundamentals of Device and Systems Packaging** (McGraw-Hill, 2019).

It covers 17 core semiconductor, packaging and system technologies and four applications of these to computing, 5G communications, automotive, and others.

- For Industry Engineers, Academic Faculty, and Postgraduate Students.
- Taught by Global Experts. Participation certificate will be issued to each student for the courses taken.
- Book and course content same.
- Each student can order a low cost Indian edition from amazon.
- 36 Hours of teaching over three months. Each student completing the course will get a certificate.
- Faculty, Students and Engineers can choose selective topics by paying for each class.

Class Duration:
Each class is about 2 hours followed by 30 min. Q&A discussion
Class Timing:
Classes start at 7.30PM IST on Saturdays and Sundays
(A total of 18 classes over three months)

Course Topics and Faculty List

- Introduction to Device and Systems Packaging
  Prof. Rao R. Tummala, Georgia Tech
- Introduction to Devices
  Prof. Abhisek Dixit, IIT Delhi
- Fundamentals of Electrical Design
  Prof. Rohit Sharma, IIT Ropar
- Fundamentals of Thermal Technologies
  Prof. Anandaroop Bhattacharya, IIT Kharagpur
- Fundamentals of Thermo-mechanical Reliability
  Prof. Ganesh Subbarayan, Purdue University
- Fundamentals of Package Materials
  Dr. Ravi Bhatkal, MacDermid Alpha India
- Fundamentals of Package Substrates
  Dr. Venky Sundaram, 3D System Scaling LLC
- Fundamentals of Passive Components and Their Integration
  Prof. Raj Pulugurtha, Florida International University
- Fundamentals of Chip-to-Package Interconnect. & Assembly
  Prof. Vanessa Smet, Georgia Tech
- Fundamentals of Embedded & Fan Out Packaging
  Dr. Beth Keser, Zero ASIC
- Fundamentals of 3D Packaging With and without TSV
  Dr. Siddharth Ravichandran, Chipletz
- Fundamentals of RF and Millimeter-wave Packaging
  Prof. Emmanouil M Tentzeris, Georgia Tech
- Fundamentals of Opto-electronics packaging
  Dr. Ajey Jacobs, USC
- Fundamentals of MEMS and Sensors packaging
  Prof. Venkatesh KP Rao, BITS Pilani
- Fundamentals of Encapsulation, Molding & Sealing
  Dr. Jack Moon, Georgia Tech
- Fundamentals of Printed Wiring Boards
  Dr. Sundar Kamath, Sanmina
- Fundamentals of Board Assembly
  Prof. Nilesh Badwe, IIT Kanpur
- Power Electronics
  Prof. Shiladri Chakraborty, IIT Bombay

Scan Code for details on course structure, schedule and fees or please visit: https://crest.bits-pilani.ac.in/pdc

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IDSPS Technology Workforce education programs

- **Short-term:**
  - Identify course curriculum needs - Done
  - Develop graduate-level theory course on WBG power devices, systems, and packaging – In Progress
  - Knowledge acquisition: webinars, in-person expert workshops - Done

Past Expert webinars organized last year by Power Electronics SRA (2023)

Date	Speaker	Topic
July 12	Dr. Madhur Bobde (CTO - Alpha Omega)	Superjunction Power Devices
Aug 21	Prof. Vanessa Smet (Georgia Tech.)	Power modules - Thermal Management, Reliability, Substrates
Aug 22	Dr. Sreekant Narumanchi (NREL)	Thermal Management of Power Electronics
Aug 24	Dr. Shailesh Joshi (Toyota)	Automotive power electronics - Thermal Management
Aug 25	Prof. Alan Mantooth (Univ. of Arkansas)	Power Electronics Packaging
Aug 25	Dr. Madhusudan Iyengar (Google)	Thermal Challenges in Computing Platforms
Aug 26	Dr. Ritu Sodhi (Ex-ROHM, Fairchild, IR)	Power Semiconductor Devices
Sep 4	Dr. Brij Singh (John Deere)	Power Electronics for Off-Road Electric Vehicles

Technology Workforce education programs

- **Short-term:**

Recent Workshop on Power Electronics Packaging

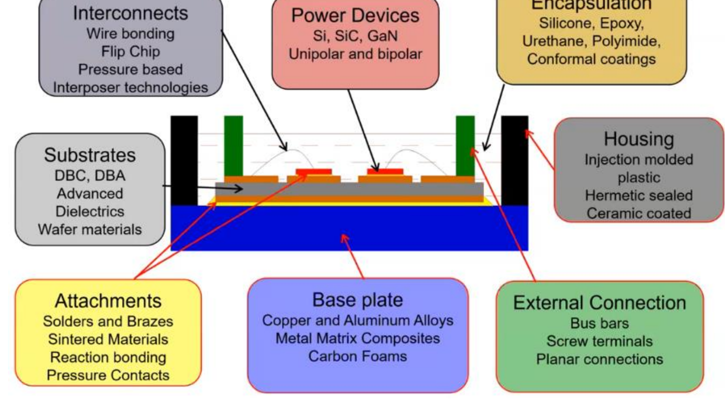
IIT Bombay welcomes all attendees to

Workshop on "Packaging and Integration of Power Electronics"

Funded by: IIT Bombay Institution of Eminence (IOE) Cell

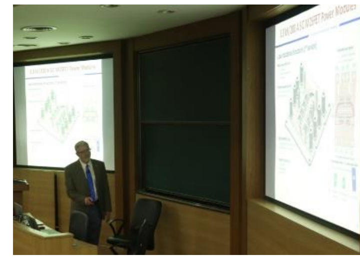
August 08 ,2024 | 10 :00 AM – 5:00 PM.

Victor Menezes Convention Centre (VMCC), IIT Bombay
Lecture Hall - 21



Sessions

- ***Fundamentals of power electronics packaging,*** Prof. Alan Mantooth
- ***State-of-the-art power packaging approaches,*** Prof. Shiladri Chakraborty, EE, IIT B
- ***Advanced packaging solutions for power electronics,*** Ravi Bhatkal, MacDermid Alpha
- ***Advanced gate-drive techniques for SiC switches,*** Prof. Sandeep Anand, EE, IIT B
- ***Design automation and future trends in power packaging,*** Prof. Alan Mantooth



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IDSPS Technology Workforce education programs

- **Long-term:**
  - ***Educated workforce target*** **over 5 (10) years – B.Tech.- 75 (150), M.Tech.- 50 (100), Ph.D.- 20 (75)**
  - Convert graduate-level course to MOOC
    - e.g., NPTEL, Coursera
  - Hands-on lab for students/ industry professionals on design, assembly, and testing
    - e.g., CAD, FEA, substrate development, wire & precision bonding, encapsulation, imaging (SEM, SAM, XCT) use of probe station & curve tracer, reliability testing
  - Technicians' training of use of equipment
  - Month-long hands-on training of students at US collaborating institutions through short-term govt.-sponsored student exchange mobility grants
    - e.g., SPARC
  - Global annual Ph.D. virtual summer school on power packaging
    - e.g., IEEE Power Electronics Society

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IDSPS Power Electronics SRA: Five-Year Plan

	Year 1	Year 2	Year 3	Year 4	Year 5
Submit Proposal	■				
Identify industry partners	■				
Set up industry consortium	■	■			
Set up infrastructure		■	■		
Develop Research Programs		■	■	■	■
Develop Educational Programs		■	■	■	■
Demonstrate Technologies			■	■	■
Integrate Technologies into Industry Prototype 1			■	■	■
Integrate Technologies into Industry Prototype 2				■	■
Integrate Technologies into Industry Prototype 3					■

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The IDSPS Power Electronics SRA needs cross-disciplinary research...

Please reach out at shiladri@ee.iitb.ac.in, apurv@ee.iitr.ac.in

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